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(54) **METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE**

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(57) **ABSTRACT**

In a semiconductor device in which a channel formation region is included in an oxide semiconductor layer, an oxide insulating film below and in contact with the oxide semiconductor layer and a gate insulating film over and in contact with the oxide semiconductor layer are used to supply oxygen of the gate insulating film, which is introduced by an ion implantation method, to the oxide semiconductor layer.

14 Claims, 23 Drawing Sheets

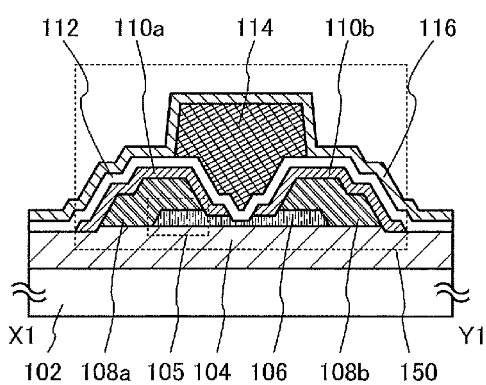

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FIG. 1A

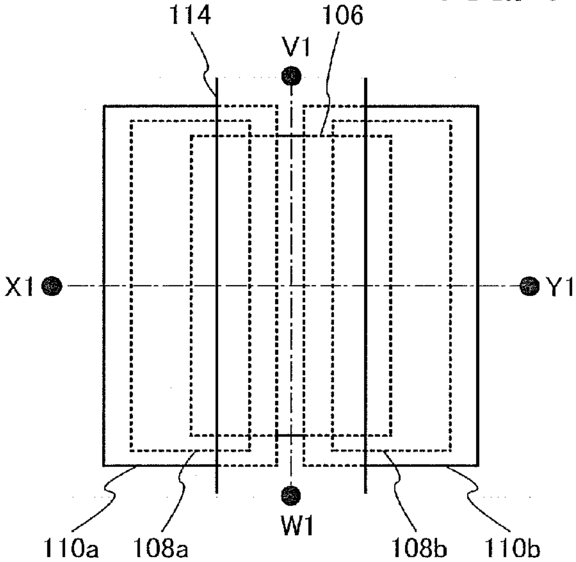


FIG. 1C

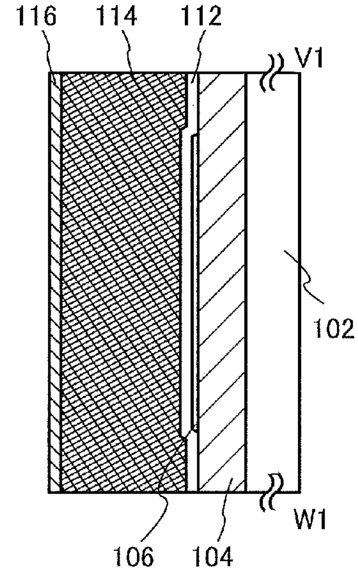


FIG. 1B

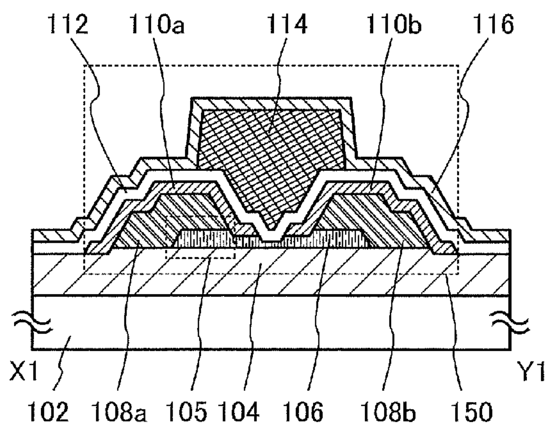


FIG. 1D

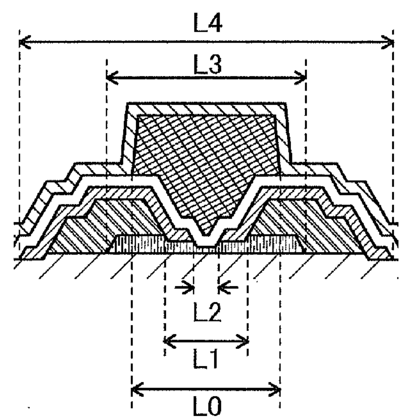


FIG. 1E

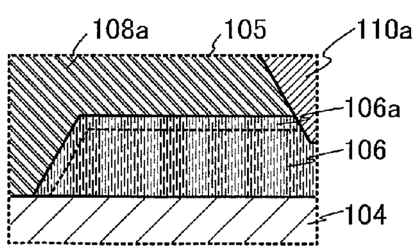


FIG. 2A

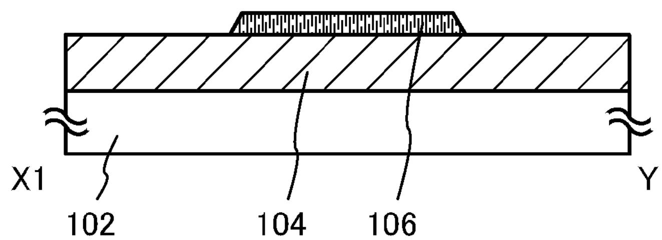


FIG. 2B

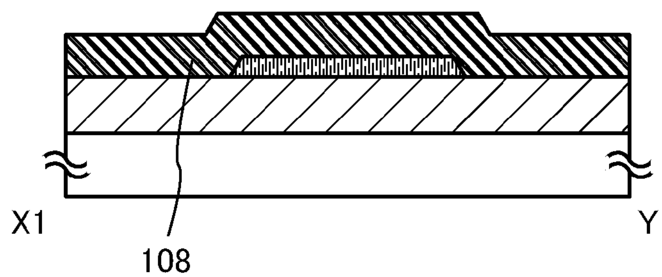


FIG. 2C

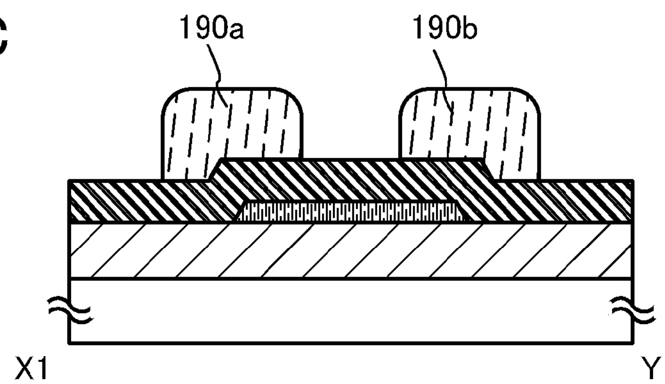


FIG. 2D

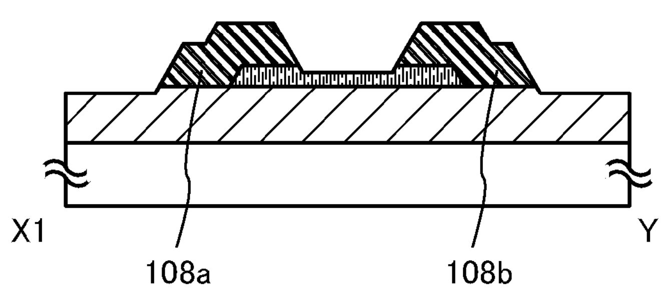


FIG. 3A

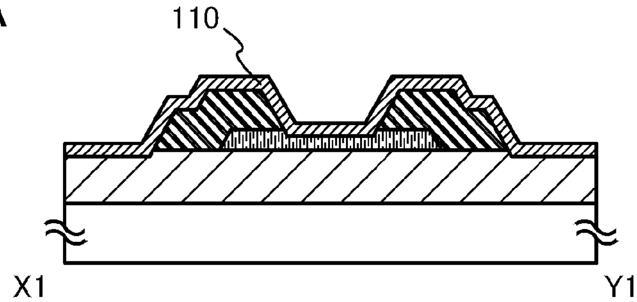


FIG. 3B

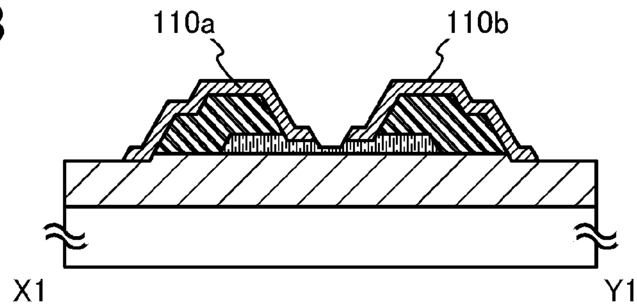


FIG. 3C

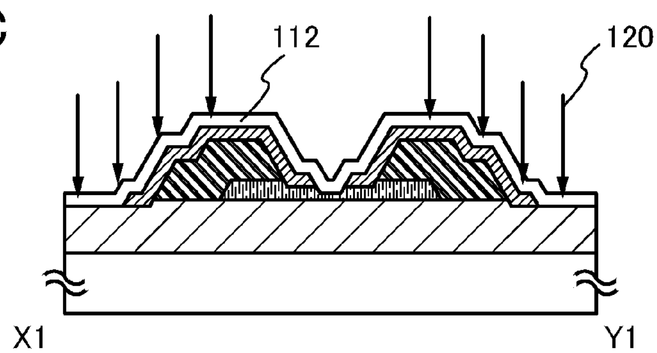


FIG. 3D

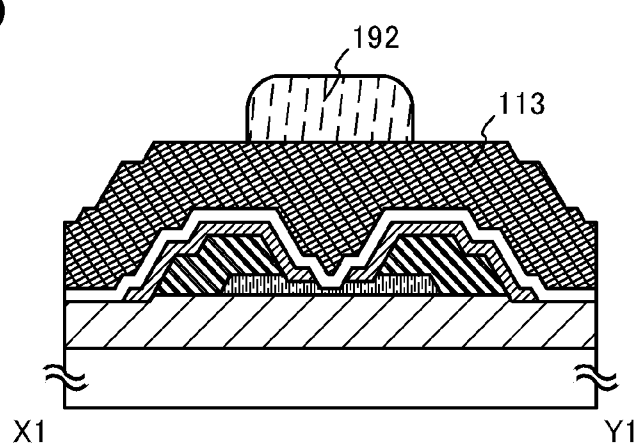


FIG. 4A

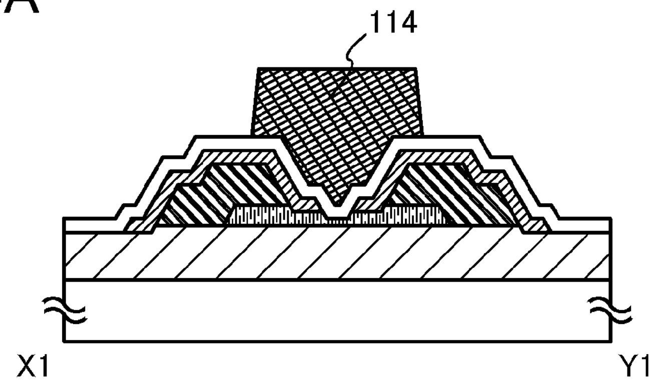


FIG. 4B

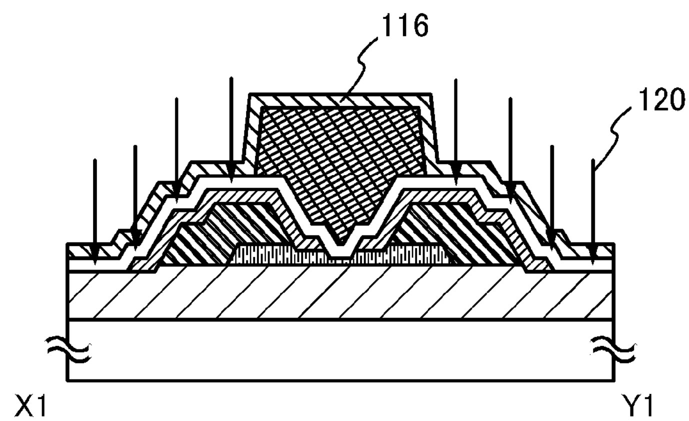


FIG. 4C

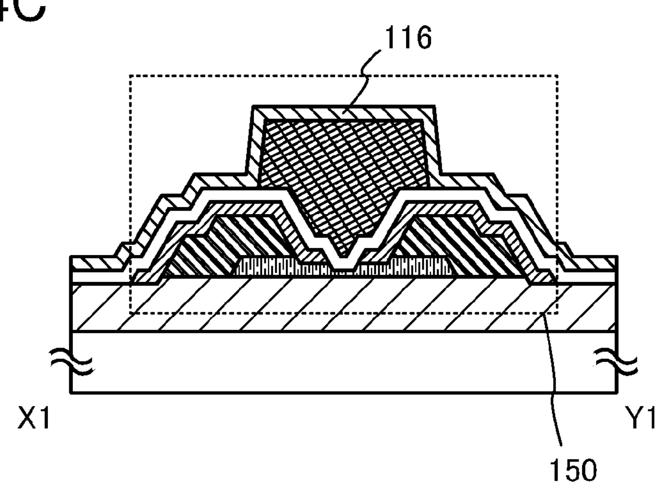


FIG. 5A

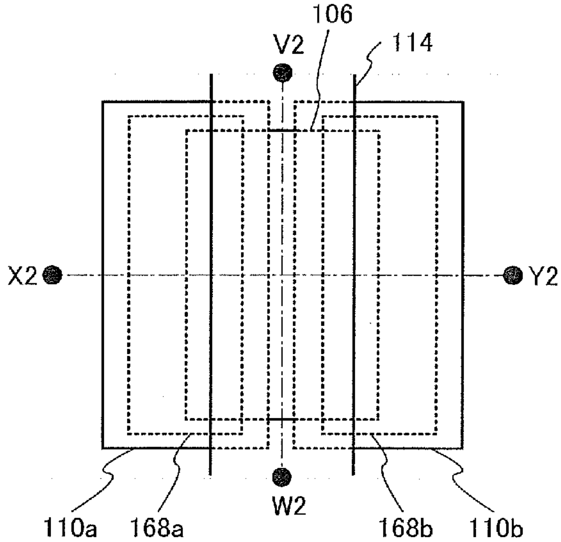


FIG. 5C

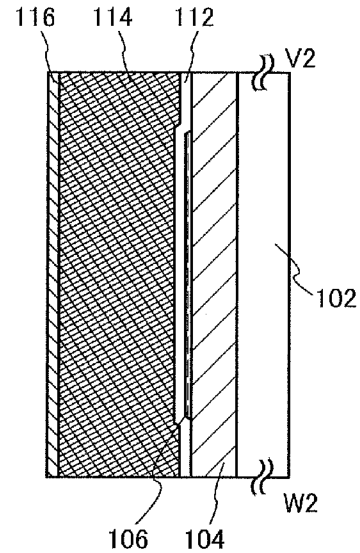


FIG. 5B

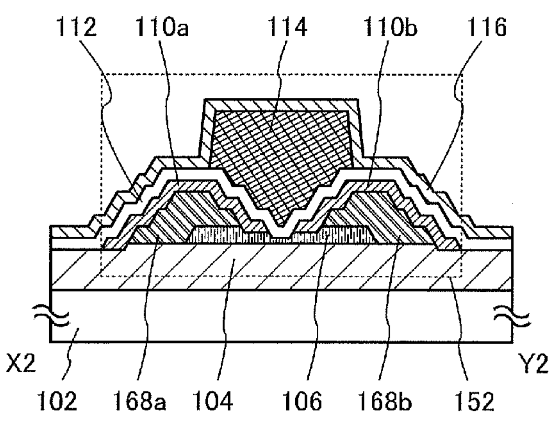


FIG. 6A

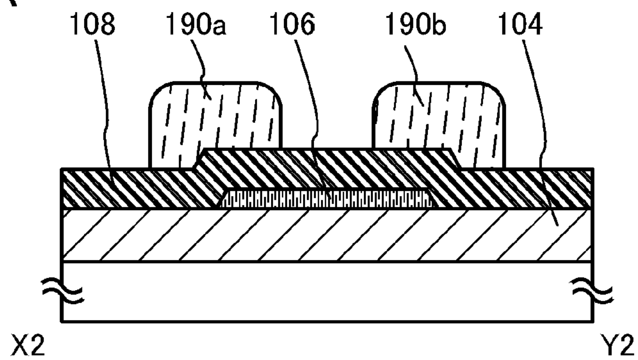


FIG. 6B

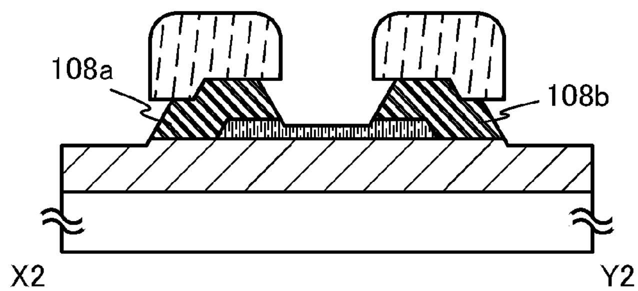


FIG. 6C

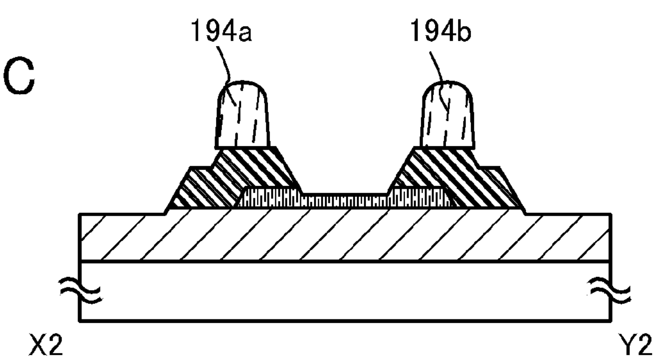


FIG. 6D

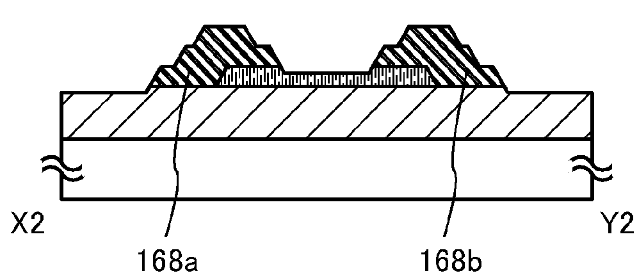


FIG. 7A

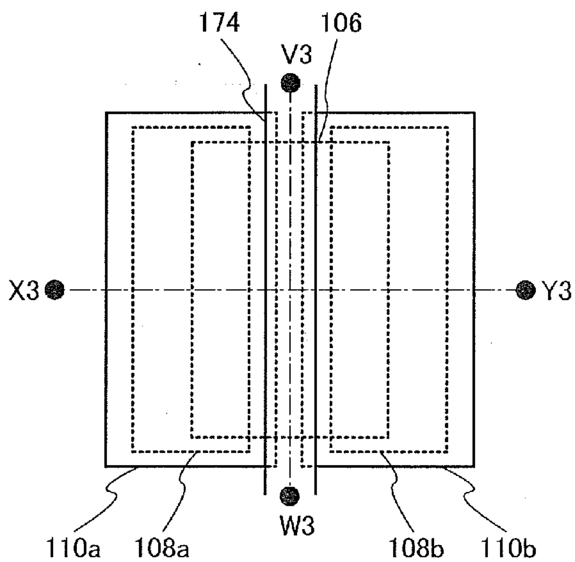


FIG. 7C

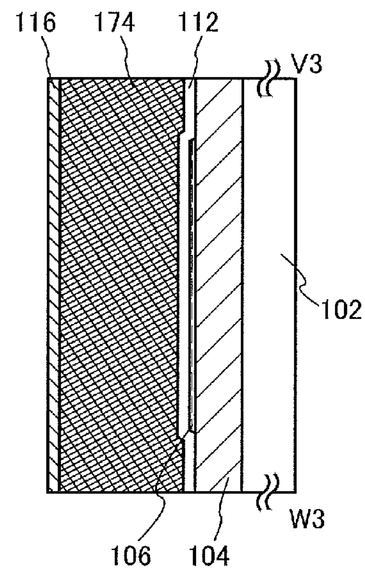


FIG. 7B

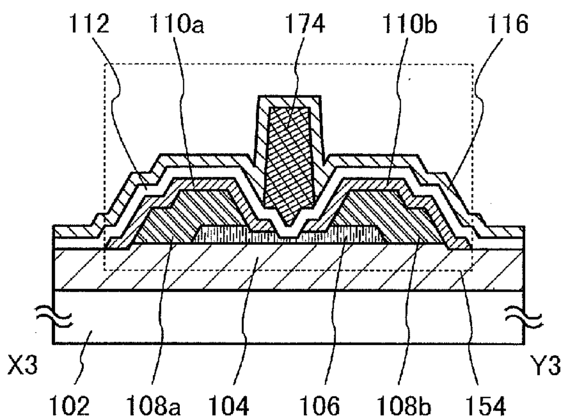


FIG. 7D

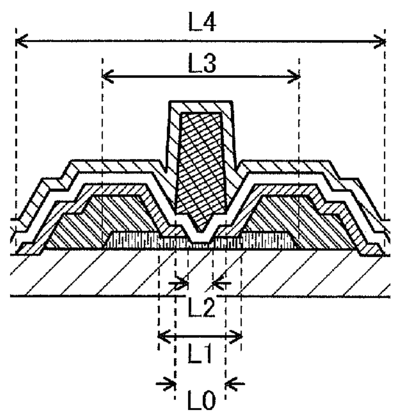


FIG. 8A

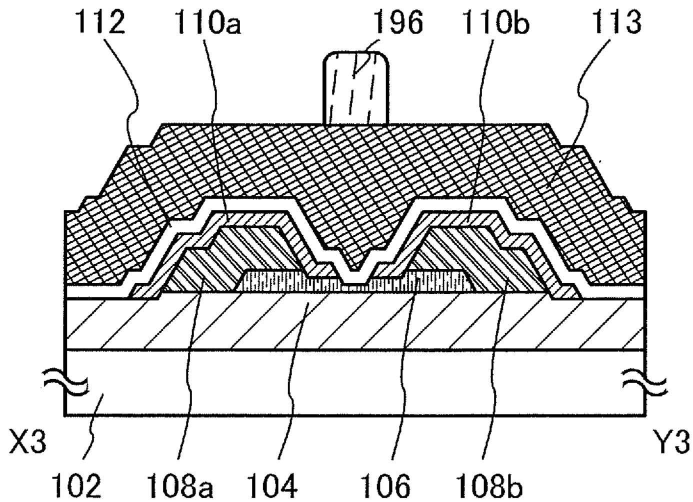


FIG. 8B

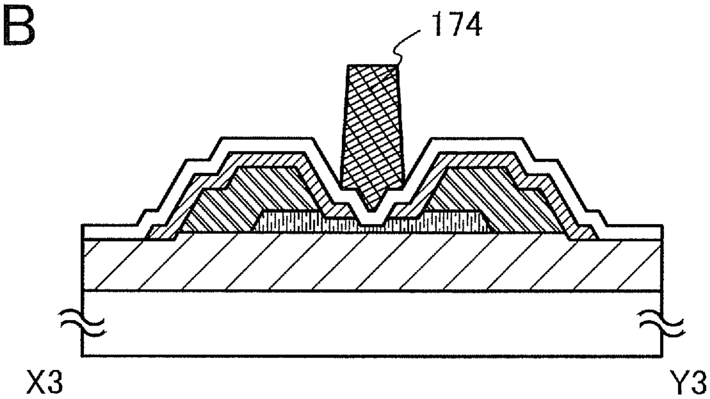


FIG. 9A

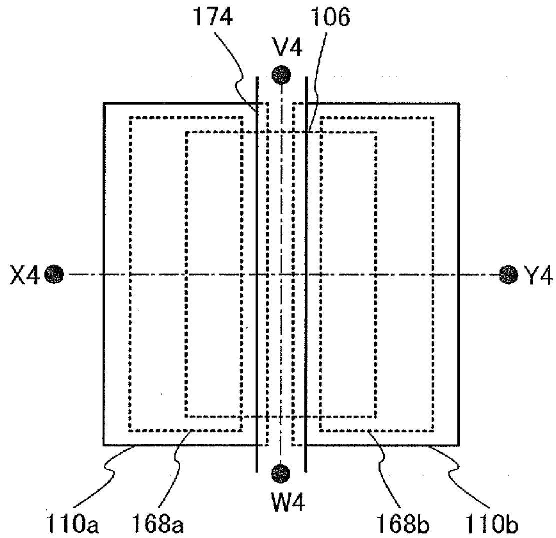


FIG. 9C

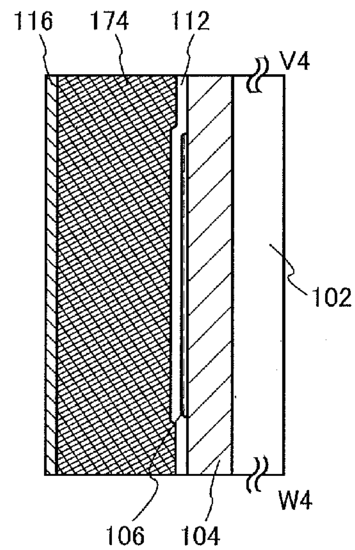


FIG. 9B

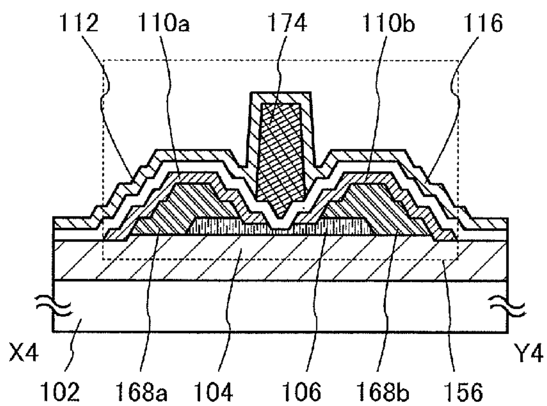


FIG. 10A

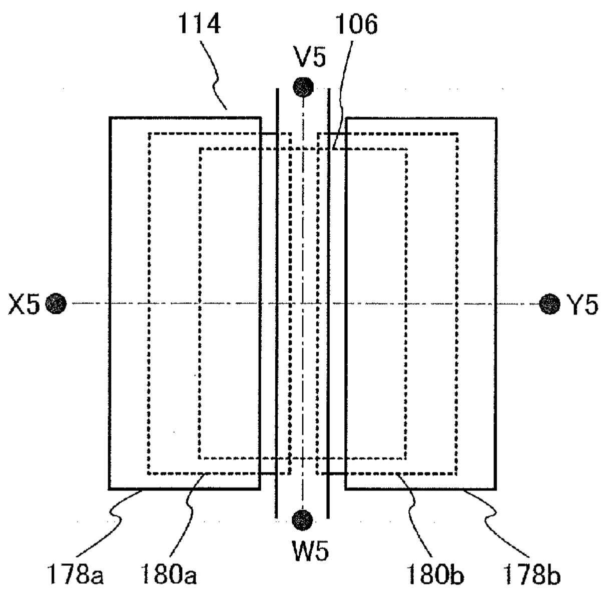


FIG. 10C

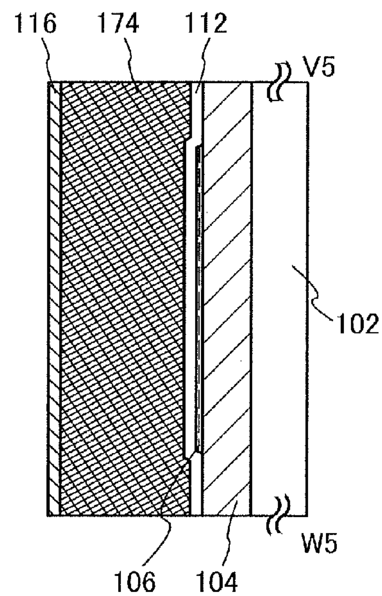


FIG. 10B

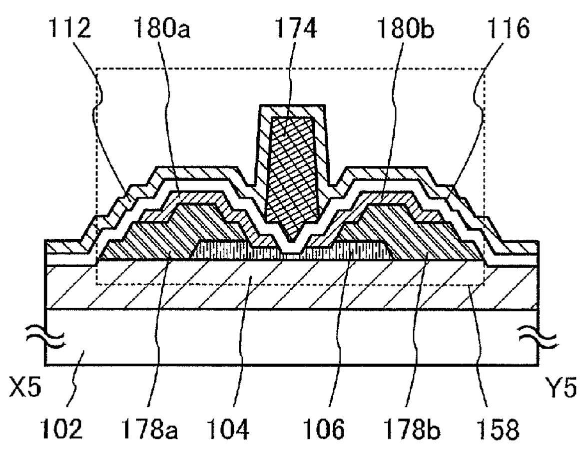


FIG. 11A

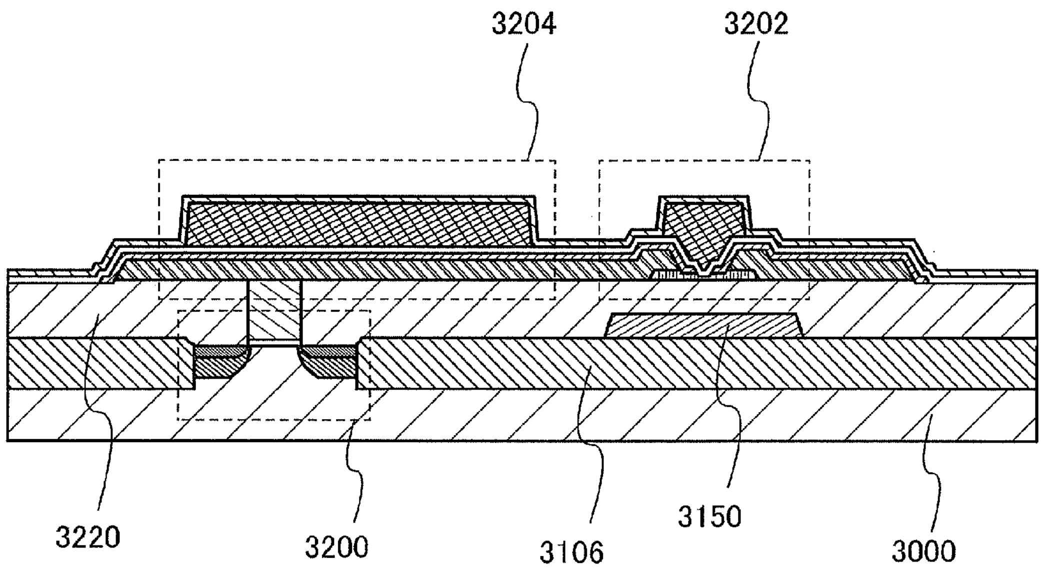


FIG. 11B

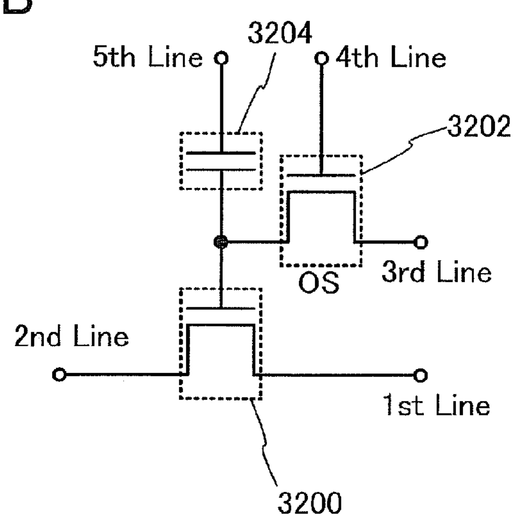


FIG. 12A

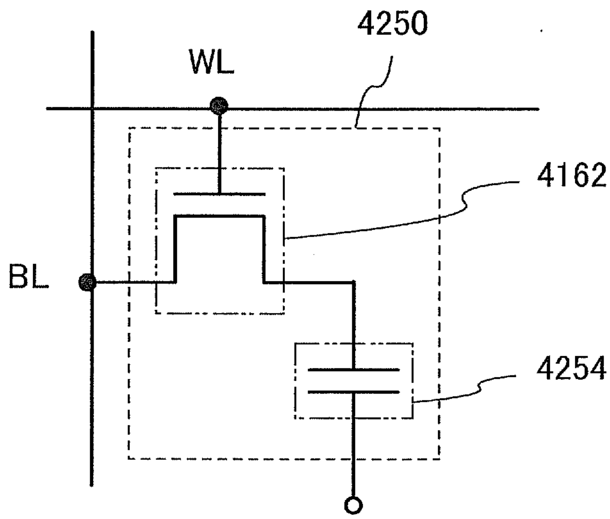


FIG. 12B

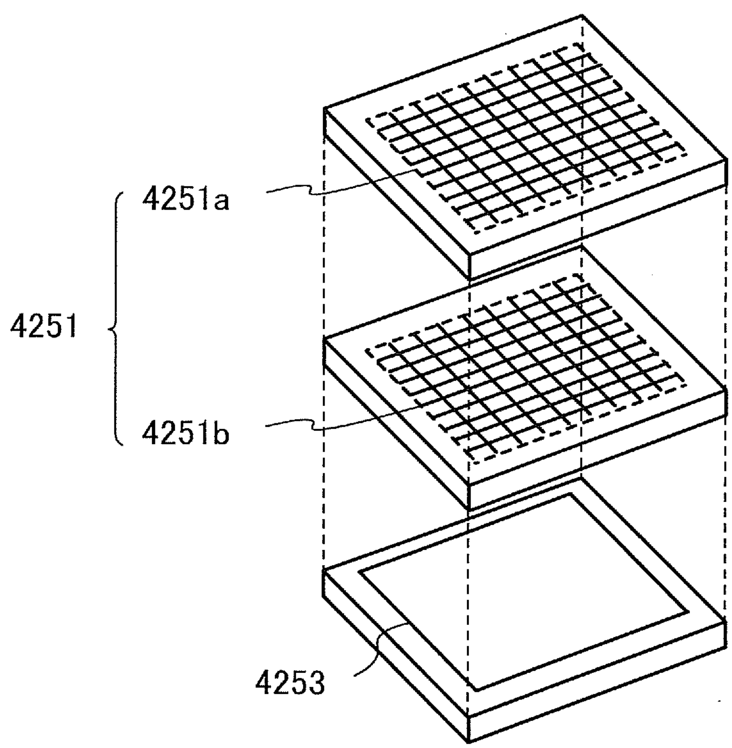
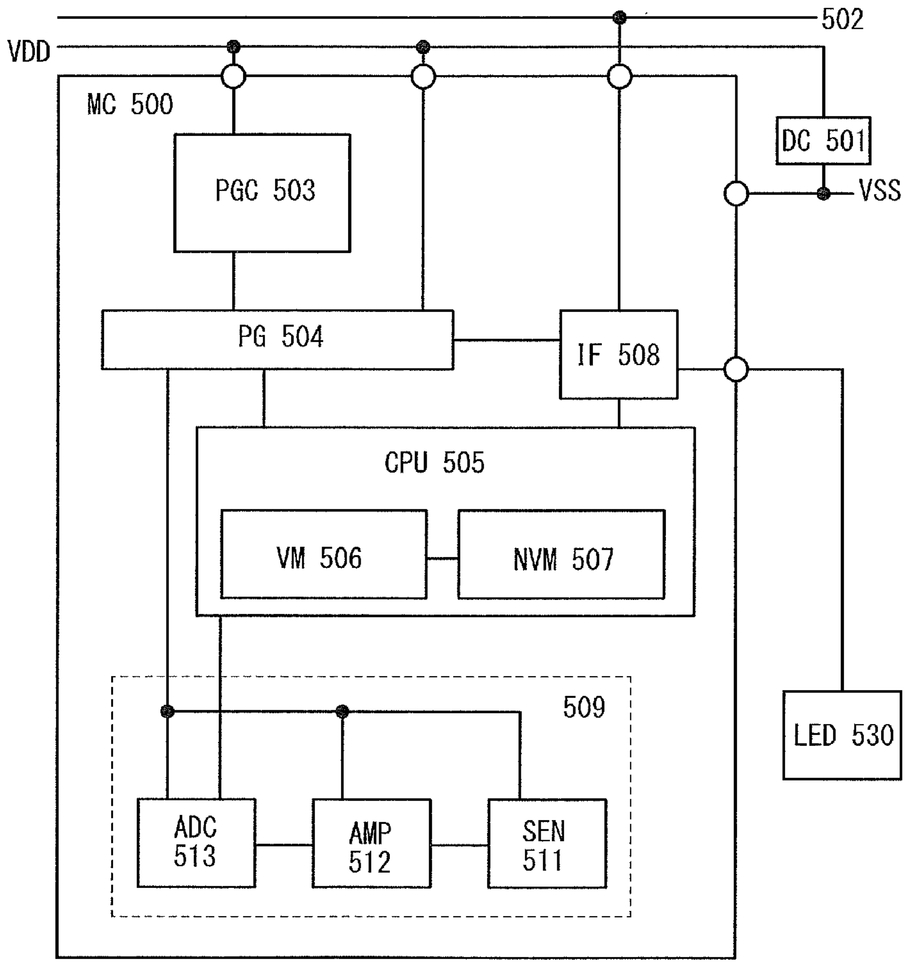


FIG. 13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LED 530
ADC
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AMP
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SEN
511

FIG. 14

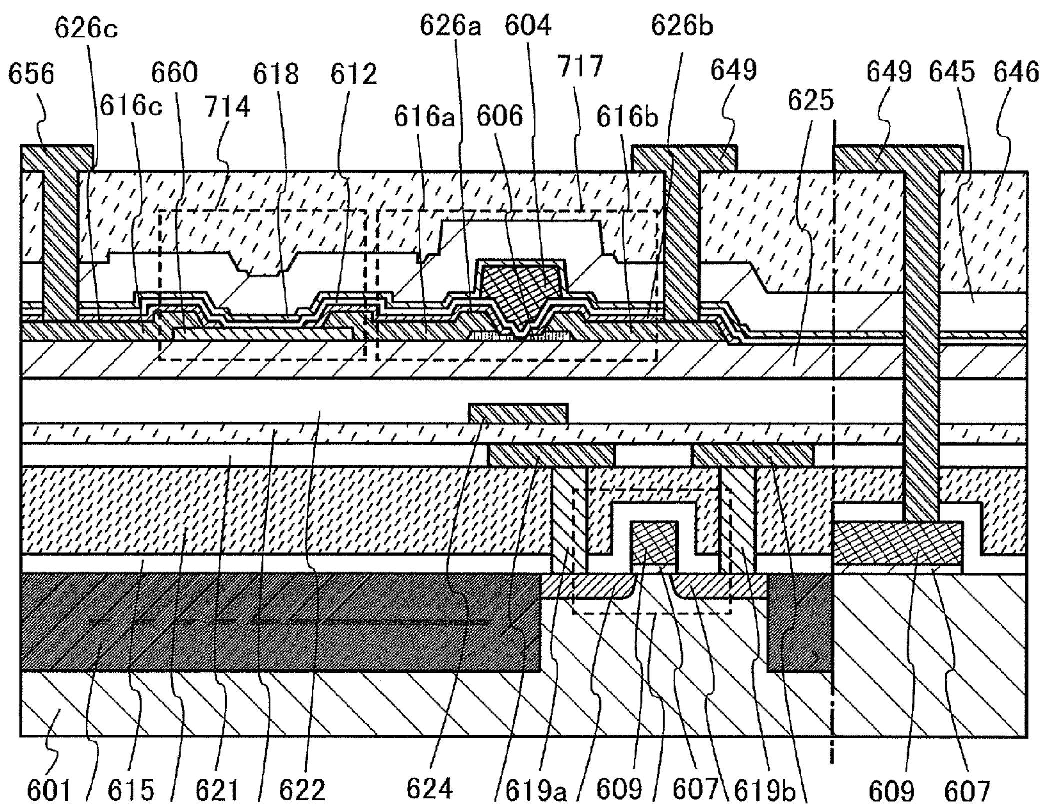
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FIG. 15A

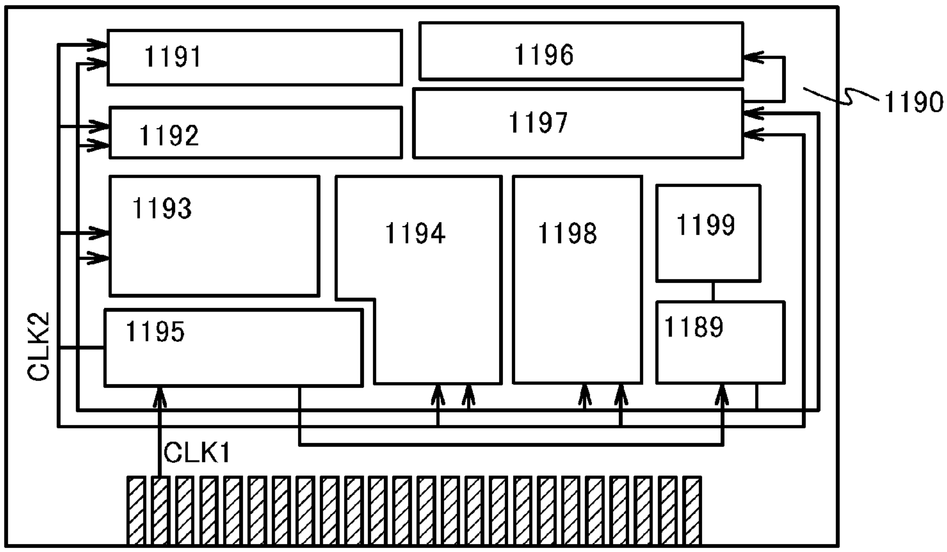


FIG. 15B

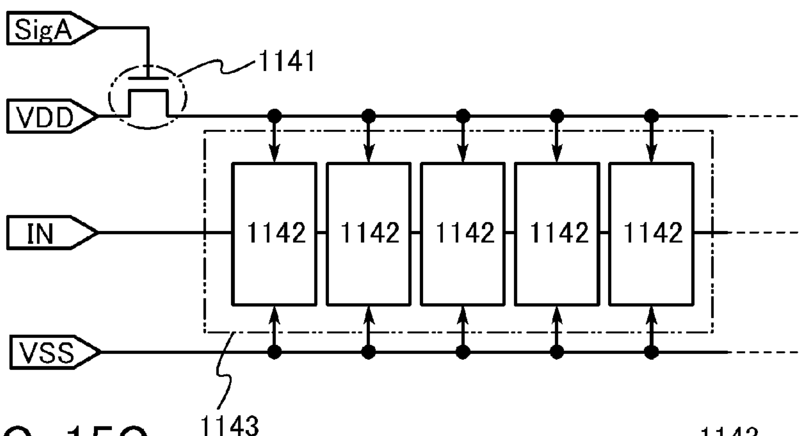


FIG. 15C

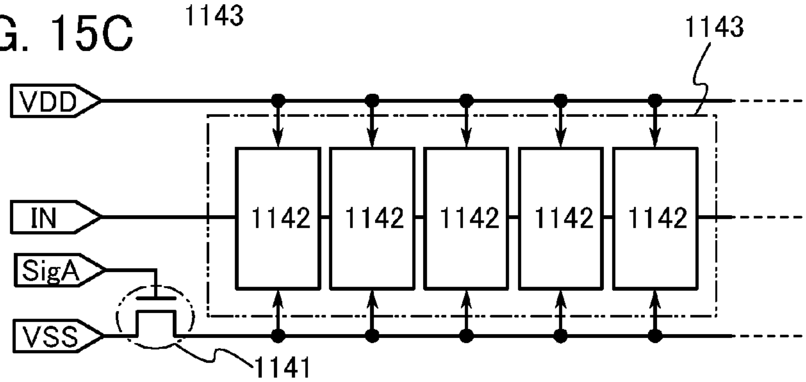


FIG. 16A

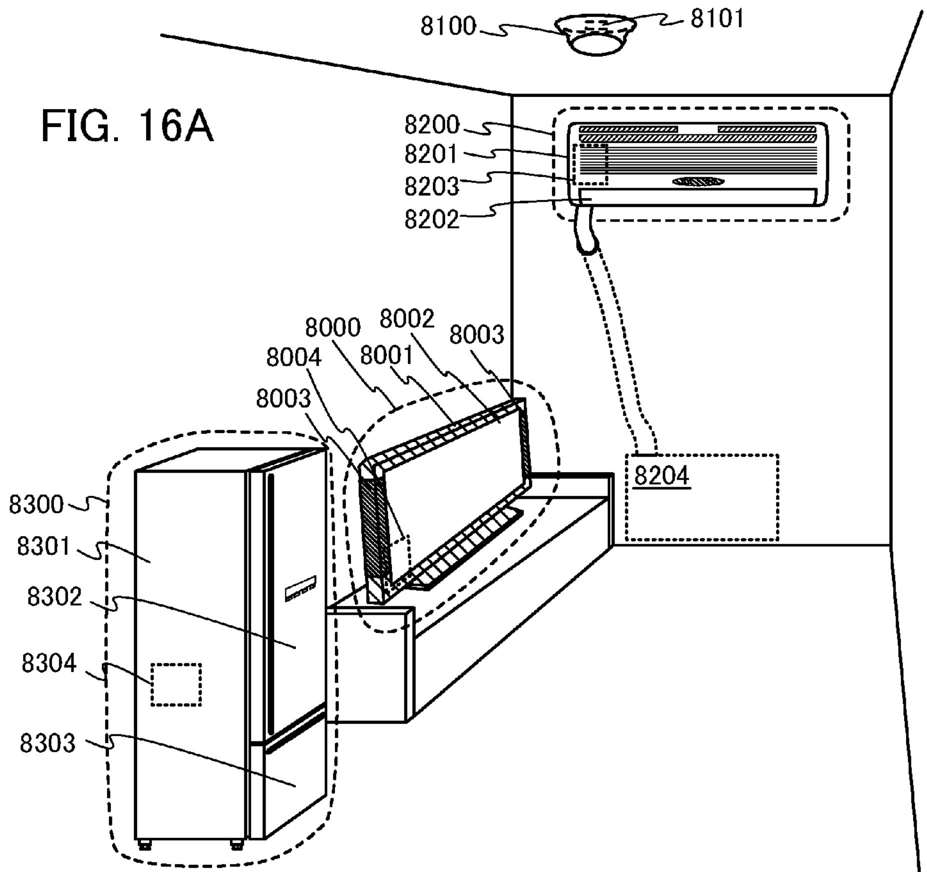


FIG. 16B

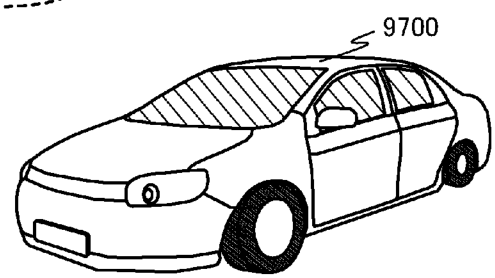


FIG. 16C

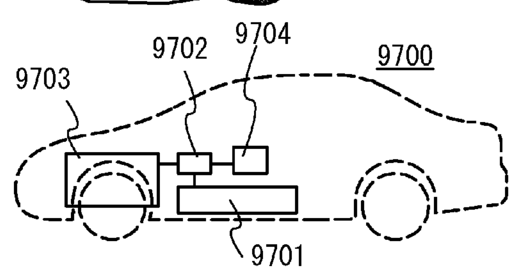


FIG. 17A

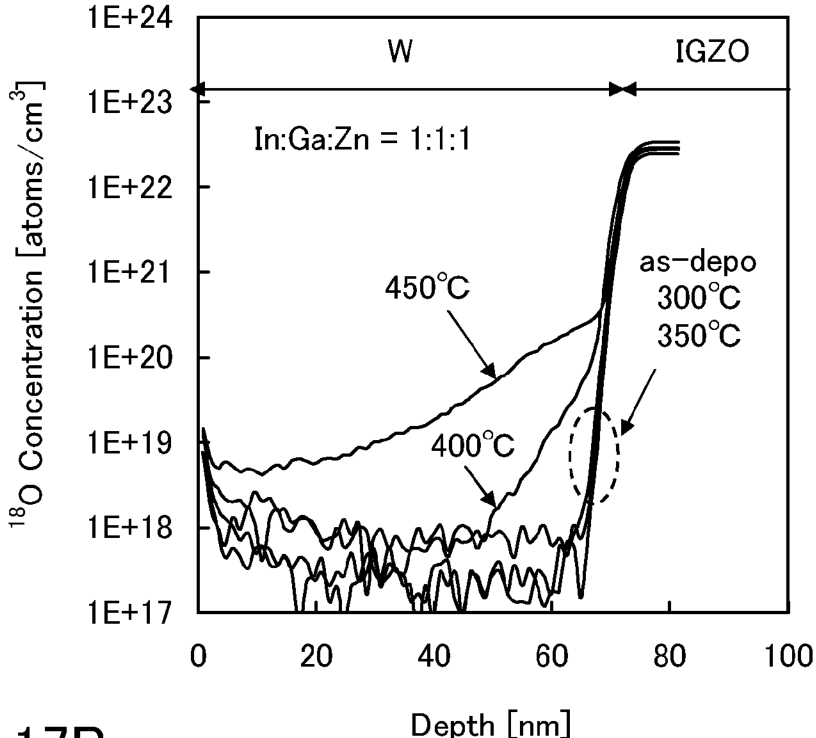


FIG. 17B

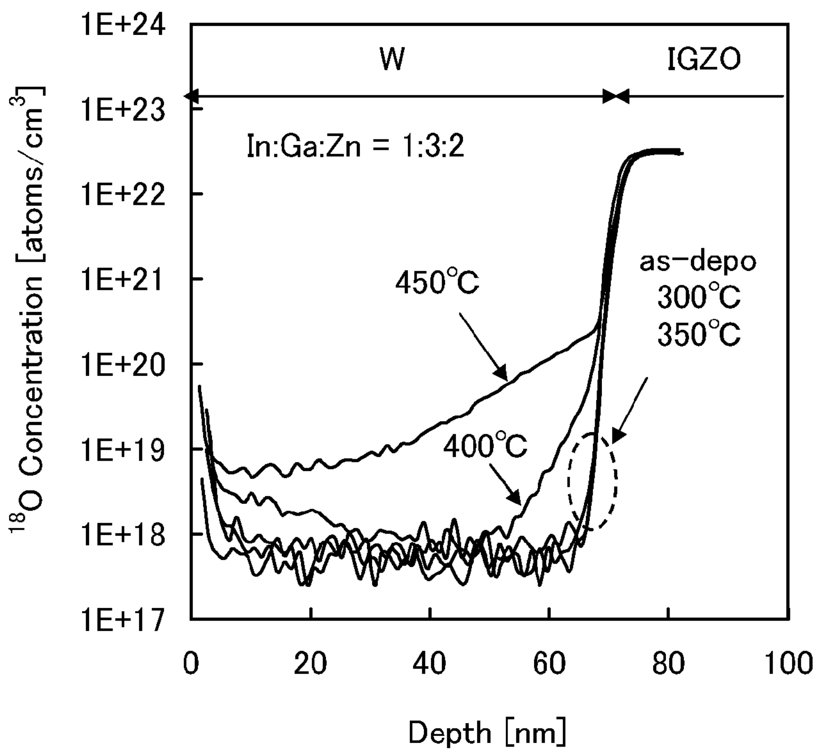


FIG. 18A

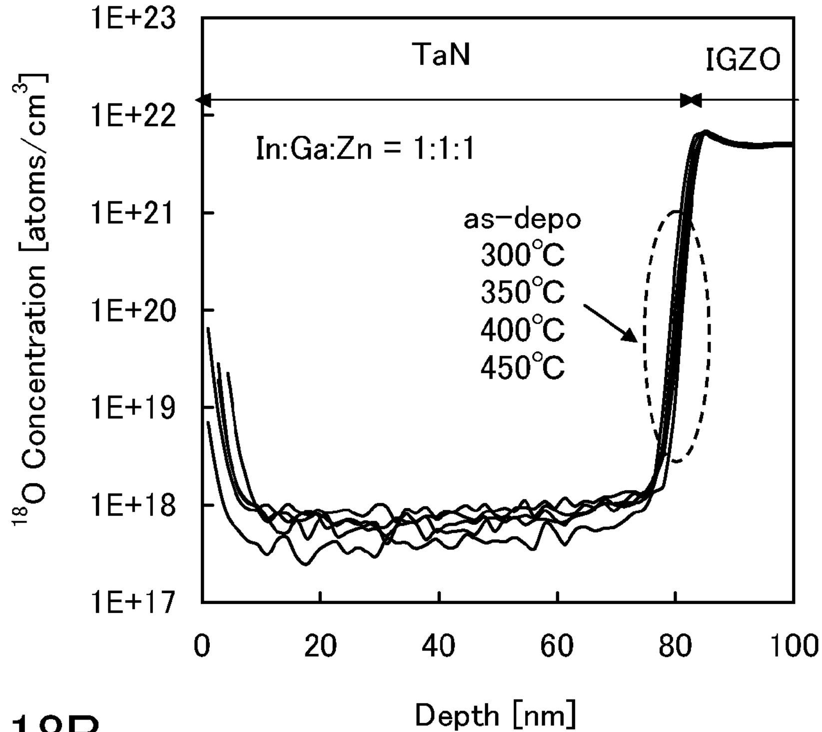


FIG. 18B

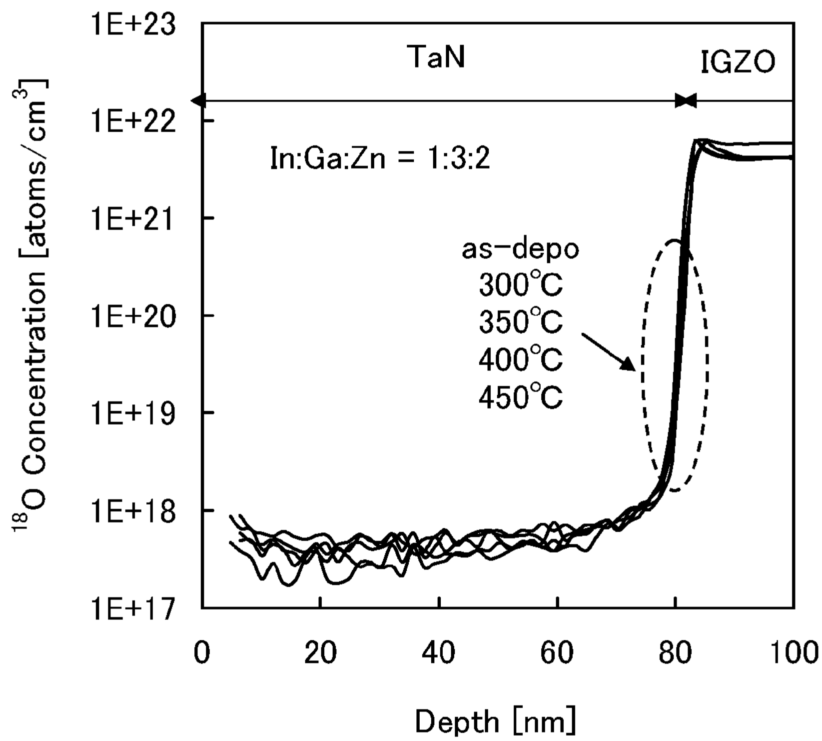


FIG. 19A

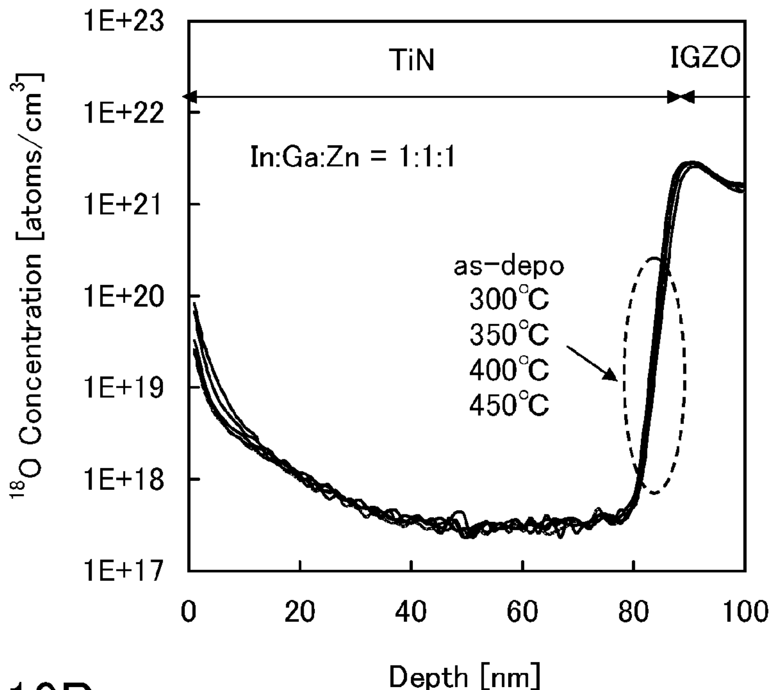


FIG. 19B

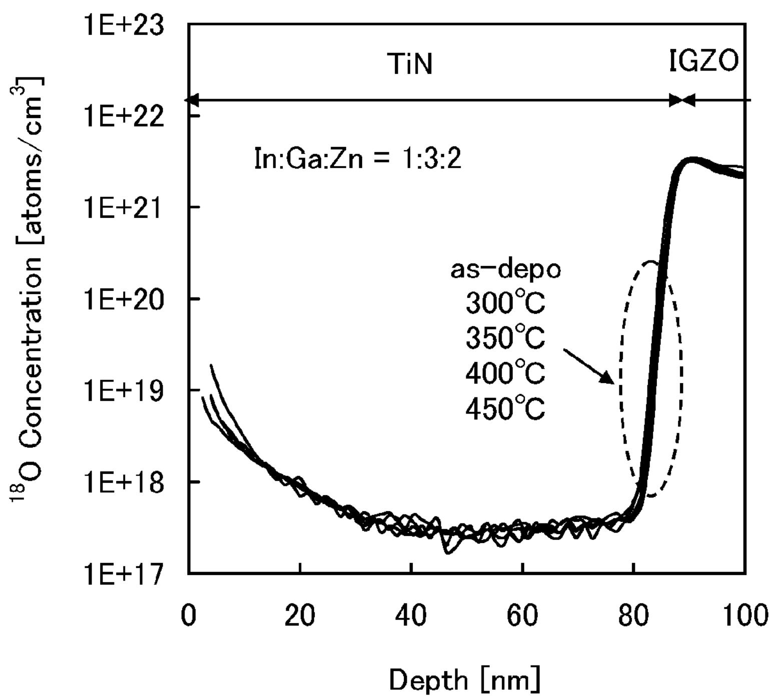


FIG. 20A

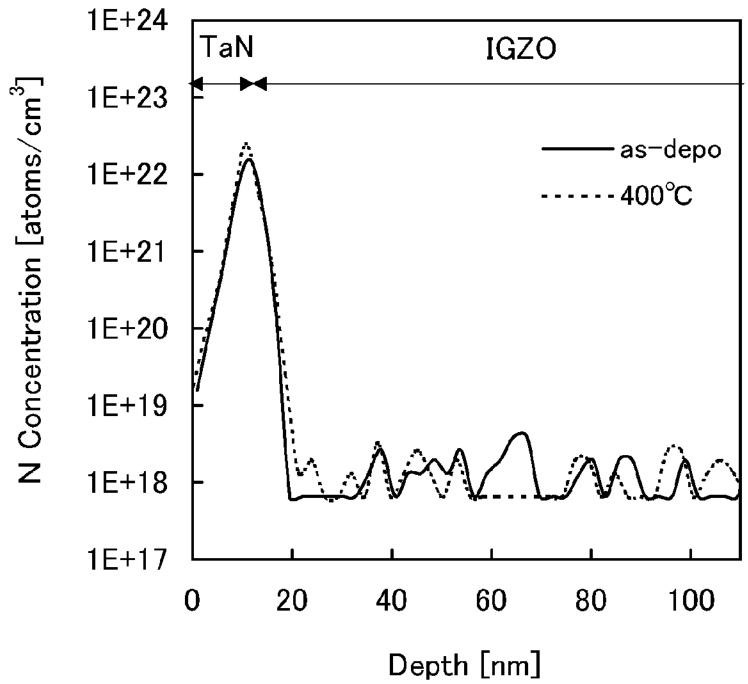


FIG. 20B

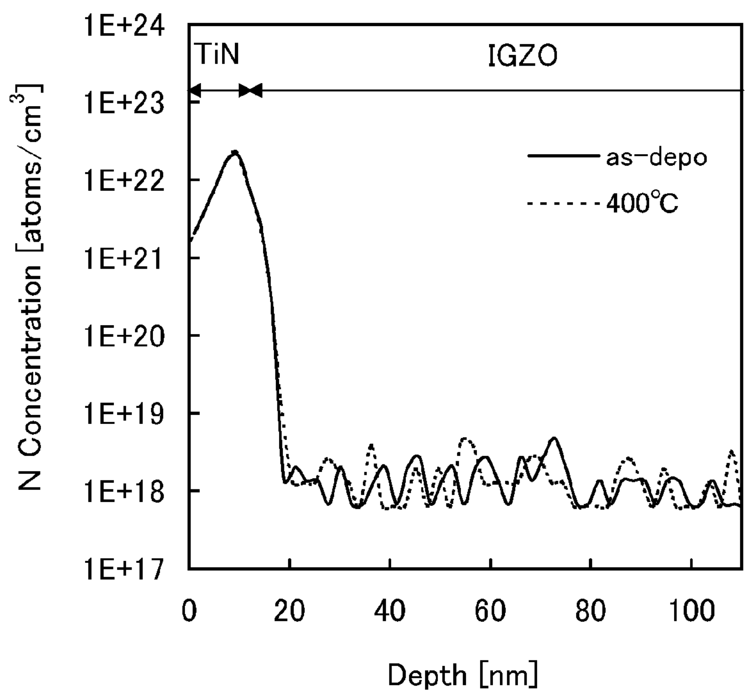


FIG. 21A

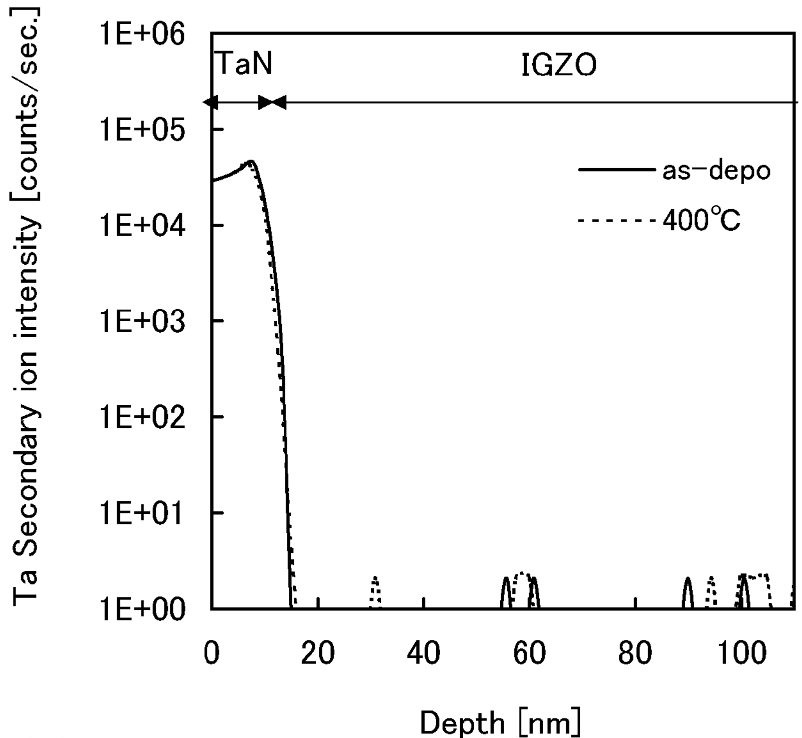


FIG. 21B

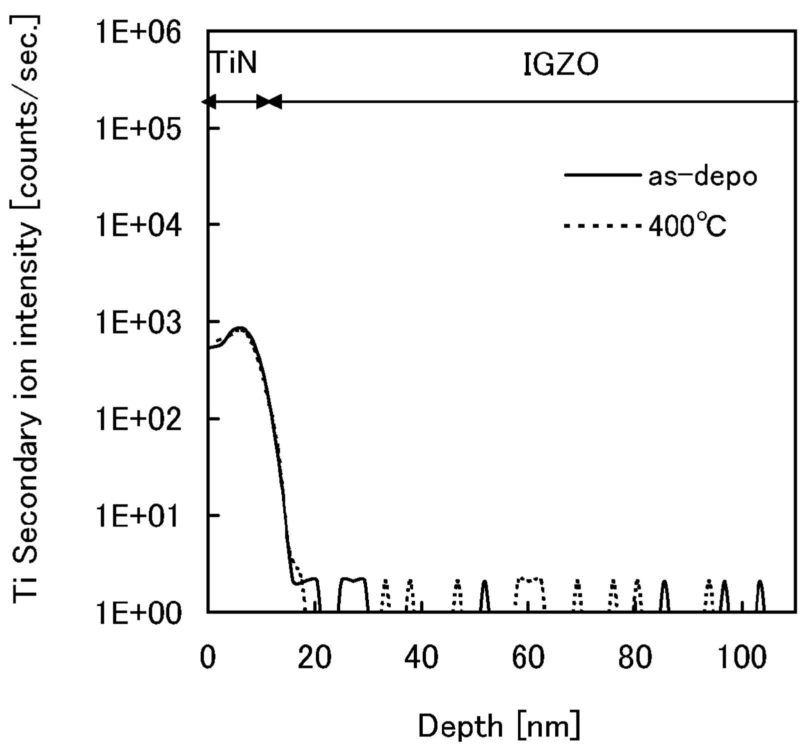


FIG. 22

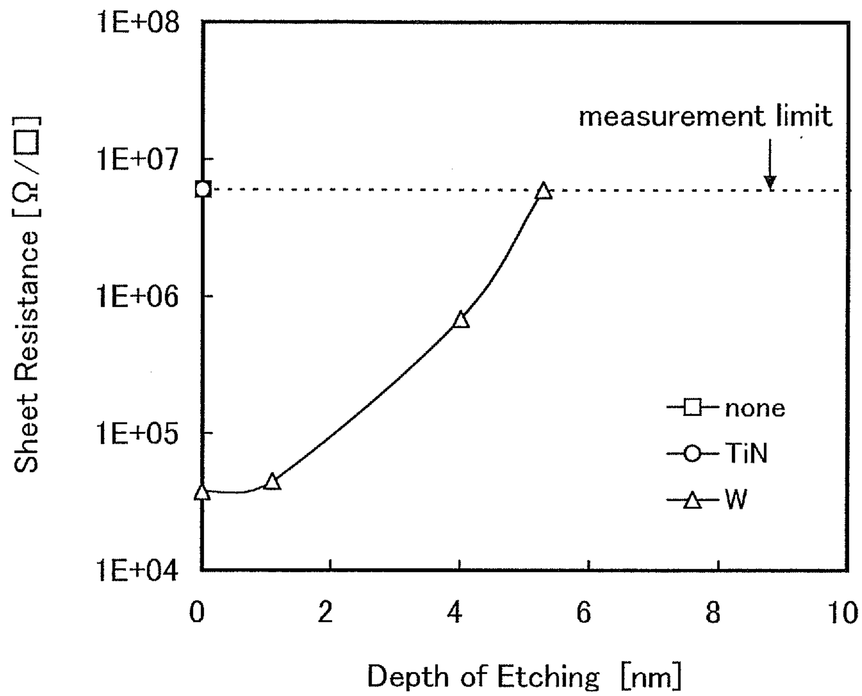

1E+08
1E+07
1E+06
1E+05
1E+04
Sheet Resistance [Ω/□]
measurement limit
none
TiN
W
0
2
4
6
8
10
Depth of Etching [nm]

FIG. 23A

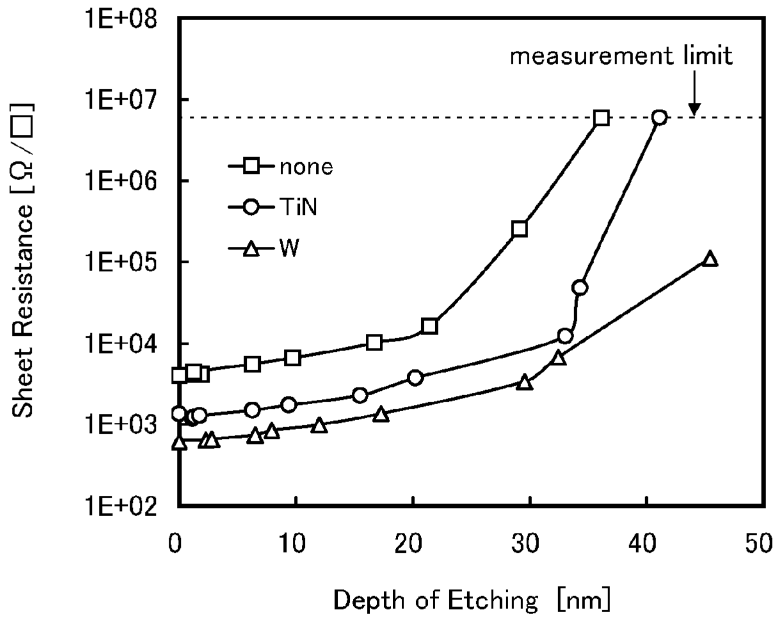
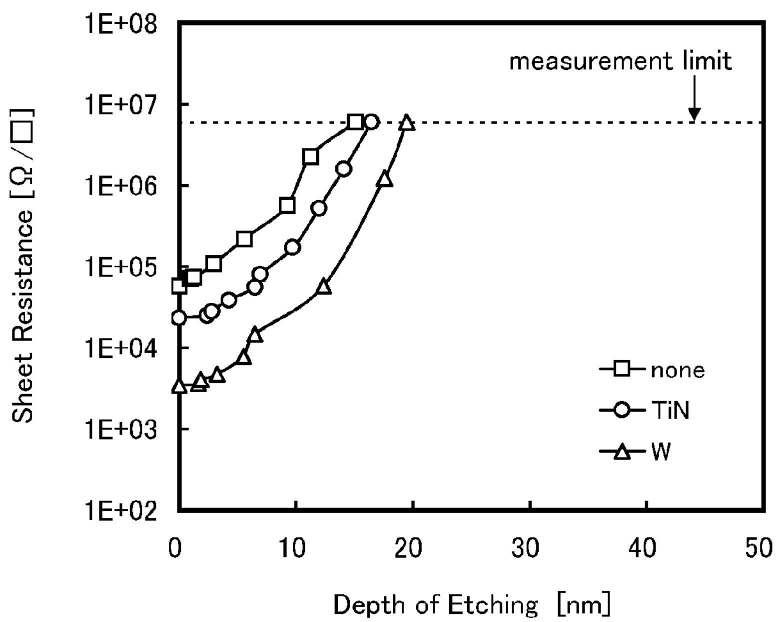


FIG. 23B



METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device including an oxide semiconductor and a method for manufacturing the semiconductor device.

In this specification, a "semiconductor device" refers to a device that can function by utilizing semiconductor characteristics; an electro-optical device, a semiconductor circuit, and an electric device are all included in the category of the semiconductor device.

2. Description of the Related Art

Attention has been focused on a technique for forming a transistor using a semiconductor thin film formed over a substrate having an insulating surface (also referred to as a thin film transistor (TFT)). The transistor is applied to a wide range of electronic devices such as an integrated circuit (IC) or an image display device (display device). A silicon-based semiconductor material is widely known as a material for a semiconductor thin film applicable to a transistor. As another material, an oxide semiconductor has been attracting attention.

For example, a transistor whose active layer includes an amorphous oxide semiconductor containing indium (In), gallium (Ga), and zinc (Zn) is disclosed (see Patent Document 1).

REFERENCE

Patent Document

[Patent Document 1] Japanese Published Patent Application No. 2006-165528

SUMMARY OF THE INVENTION

It is known that an oxygen vacancy in an oxide semiconductor becomes a donor; thus, in the case where the oxide semiconductor is used for a channel formation region of a transistor, an oxide semiconductor layer including as few oxygen vacancies as possible is preferably used.

However, even when an oxide semiconductor layer includes few oxygen vacancies initially, oxygen vacancies will increase in number from various causes. An increase in oxygen vacancies in an oxide semiconductor layer causes poor electrical characteristics in some cases; for example, the transistor becomes normally-on, leakage current increases, or threshold voltage is shifted due to stress application.

Thus, an object of one embodiment of the present invention is to provide a semiconductor device in which an increase in oxygen vacancies in an oxide semiconductor layer can be suppressed. Another object is to provide a semiconductor device with favorable electrical characteristics. In addition, another object is to provide a highly reliable semiconductor device.

According to one embodiment of the present invention, in a semiconductor device in which a channel formation region is included in an oxide semiconductor layer, an oxide insulating film below and in contact with the oxide semiconductor layer and a gate insulating film over and in contact with the oxide semiconductor layer are used to supply oxygen of the oxide insulating film or the gate insulating film to the oxide semiconductor layer. Further, a conductive nitride is used for metal films of a source electrode layer and a drain electrode layer, whereby diffusion or transfer of oxygen to the metal films is suppressed. Details thereof will be described below.

One embodiment of the present invention is a method for manufacturing a semiconductor device including a step of forming an oxide semiconductor layer over an oxide insulating film; a step of forming a first source electrode layer and a first drain electrode layer over and in contact with the oxide semiconductor layer; a step of forming a second source electrode layer and a second drain electrode layer to cover the first source electrode layer and the first drain electrode layer and be in contact with the oxide semiconductor layer; a step of forming a gate insulating film over the oxide insulating film, the oxide semiconductor layer, the second source electrode layer, and the second drain electrode layer; a step of introducing oxygen to the gate insulating film; and a step of supplying the oxygen in the gate insulating film to the oxide semiconductor layer.

In the above manufacturing method, as a method for introducing oxygen into the gate insulating film, an ion implantation method or the like may be used. Further, before oxygen is introduced into the gate insulating film, a gate electrode may be formed over the gate insulating film. Alternatively, a gate electrode may be formed over the gate insulating film, and a protective insulating film may be formed over the gate electrode before oxygen is introduced into the gate insulating film, and then oxygen may be introduced into the gate insulating film through the protective insulating film.

A structure obtained by the above method for manufacturing a semiconductor device is also one embodiment of the present invention. The structure of the semiconductor device includes an oxide insulating film; an oxide semiconductor layer over the oxide insulating film; a first source electrode layer and a first drain electrode layer in contact with the oxide semiconductor layer; a second source electrode layer and a second drain electrode layer which cover the first source electrode layer and the first drain electrode layer and are in contact with the oxide semiconductor layer; a gate insulating film over the oxide insulating film, the oxide semiconductor layer, the second source electrode layer, and the second drain electrode layer; a gate electrode layer over the gate insulating film and in a portion overlapping with the oxide semiconductor layer; and a protective insulating film over the gate insulating film and the gate electrode layer. In the semiconductor device, the gate insulating film is partly in contact with the oxide insulating film so as to cover the second source electrode layer and the second drain electrode layer.

Another embodiment of the present invention is a semiconductor device including an oxide insulating film; an oxide semiconductor layer over the oxide insulating film; a first source electrode layer and a first drain electrode layer in contact with the oxide semiconductor layer; a second source electrode layer and a second drain electrode layer in contact with the first source electrode layer and the first drain electrode layer, respectively, and in contact with the oxide semiconductor layer; a gate insulating film over the oxide insulating film, the oxide semiconductor layer, the first source electrode layer, the first drain electrode layer, the second source electrode layer, and the second drain electrode layer; a gate electrode layer over the gate insulating film and in a portion overlapping with the oxide semiconductor layer; and a protective insulating film over the gate insulating film and the gate electrode layer. In the semiconductor device, the gate insulating film is partly in contact with the oxide insulating film so as to cover the first source electrode layer and the first drain electrode layer.

In each of the above structures, the first source electrode layer and the first drain electrode layer are preferably at least one material selected from Al, Cr, Cu, Ta, Ti, Mo, and W or an alloy material containing any of these as a main component.

In each of the above structures, end portions of the first source electrode layer and the first drain electrode layer preferably have a staircase-like shape.

In each of the above structures, the second source electrode layer and the second drain electrode layer are preferably at least one material selected from tantalum nitride, titanium nitride, and ruthenium or an alloy material containing any of these as a main component.

In each of the above structures, the protective insulating film is preferably a silicon nitride film.

In each of the above structures, it is preferable that the oxide semiconductor layer contain a crystalline phase, and a c-axis of the crystalline phase be parallel to a normal vector of a surface of the oxide semiconductor layer.

In one embodiment of the present invention, a semiconductor device in which an increase in oxygen vacancies in an oxide semiconductor layer is suppressed can be provided. Further, a semiconductor device with favorable electrical characteristics can be provided. Further, a highly reliable semiconductor device can be provided.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1**A to **1**E are a top view and cross-sectional views which illustrate a semiconductor device.

FIGS. **2**A to **2**D illustrate a method for manufacturing a semiconductor device.

FIGS. **3**A to **3**D illustrate a method for manufacturing a semiconductor device.

FIGS. **4**A to **4**C illustrate a method for manufacturing a semiconductor device.

FIGS. **5**A to **5**C are a top view and cross-sectional views which illustrate a semiconductor device.

FIGS. **6**A to **6**D illustrate a method for manufacturing a semiconductor device.

FIGS. **7**A to **7**D are a top view and cross-sectional views which illustrate a semiconductor device.

FIGS. **8**A and **8**B illustrate a method for manufacturing a semiconductor device.

FIGS. **9**A to **9**C are a top view and cross-sectional views which illustrate a semiconductor device.

FIGS. **10**A to **10**C are a top view and cross-sectional views which illustrate a semiconductor device.

FIG. **11**A is a cross-sectional view of a semiconductor device, and FIG. **11**B is a circuit diagram thereof.

FIG. **12**A is a circuit diagram of a semiconductor device, and FIG. **12**B is a perspective view thereof.

FIG. **13** is a block diagram of a semiconductor device.

FIG. **14** is a cross-sectional view of a semiconductor device.

FIGS. **15**A to **15**C are block diagrams of a semiconductor device.

FIGS. **16**A to **16**C illustrate electronic devices to which a semiconductor device can be applied.

FIGS. **17**A and **17**B show results of SIMS analysis of a stacked layer including an IGZO film and a tungsten film.

FIGS. **18**A and **18**B show results of SIMS analysis of a stacked layer including an IGZO film and a tantalum nitride film.

FIGS. **19**A and **19**B show results of SIMS analysis of a stacked layer including an IGZO film and a titanium nitride film.

FIGS. **20**A and **20**B show results of SIMS analysis of a stacked layer including an IGZO film and a tantalum nitride film and a stacked layer including an IGZO film and a titanium nitride film.

FIGS. **21**A and **21**B show results of SIMS analysis of a stacked layer including an IGZO film and a tantalum nitride film and a stacked layer including an IGZO film and a titanium nitride film.

FIG. **22** shows measurement results of sheet resistance values with respect to the depth etching to which an IGZO film is etched.

FIGS. **23**A and **23**B show measurement results of sheet resistance values with respect to the depth to which an IGZO film is etched.

DETAILED DESCRIPTION OF THE INVENTION

Embodiments and examples are described in detail with reference to the drawings. Note that the present invention is not limited to the following description and it will be readily appreciated by those skilled in the art that modes and details can be modified in various ways without departing from the spirit and the scope of the present invention. Therefore, the present invention should not be limited to the descriptions of the embodiments and the examples below. Note that, in the structures of the invention described below, in some cases, the same portions or portions having similar functions are denoted by the same reference numerals in different drawings, and the descriptions of such portions are not repeated.

In this specification, functions of a “source” and a “drain” of a transistor are sometimes replaced with each other when a transistor of opposite polarity is used or when the direction of current flowing is changed in circuit operation, for example. Thus, the terms “source” and “drain” can be used to denote the drain and the source, respectively, in this specification.

Embodiment 1

In this embodiment, a semiconductor device which is one embodiment of the present invention is described with reference to drawings.

FIGS. **1**A, **1**B, **1**C, **1**D, and **1**E are a top view and cross-sectional views which illustrate a transistor of one embodiment of the present invention. FIG. **1**A is the top view of the transistor, and a cross section taken along a dashed-dotted line **X1-Y1** in FIG. **1**A is illustrated in FIG. **1**B. A cross section taken along a dashed-dotted line **V1-W1** in FIG. **1**A is illustrated in FIG. **1**C. FIG. **1**D illustrates widths of components of the transistor which are illustrated in FIG. **1**B. FIG. **1**E is an enlarged view of a region **105** illustrated in FIG. **1**B. Note that for simplification of the drawing, some components in the top view in FIG. **1**A are illustrated in a see-through manner or not illustrated.

A transistor **150** illustrated in FIGS. **1**A, **1**B, **1**C, **1**D, and **1**E includes an oxide insulating film **104** formed over a substrate **102**; an oxide semiconductor layer **106** formed over the oxide insulating film **104**; a first source electrode layer **108***a* and a first drain electrode layer **108***b* formed over the oxide semiconductor layer **106**; a second source electrode layer **110***a* and a second drain electrode layer **110***b* formed over the first source electrode layer **108***a* and the first drain electrode layer **108***b*, respectively; a gate insulating film **112** formed over the oxide insulating film **104**, the oxide semiconductor layer **106**, the second source electrode layer **110***a*, and the second drain electrode layer **110***b*; a gate electrode layer **114** formed over the gate insulating film **112** and in a position overlapping with the oxide semiconductor layer **106**; and a protective insulating film **116** formed over the gate insulating film **112** and the gate electrode layer **114**. Note that another insulating layer, another wiring, or the like may be formed over the protective insulating film **116**.

The substrate **102** is not limited to a simple supporting substrate, and may be a substrate where another device such as a transistor is formed. In that case, at least one of the gate electrode layer **114**, the first source electrode layer **108***a*, the first drain electrode layer **108***b*, the second source electrode layer **110***a*, and the second drain electrode layer **110***b* of the transistor **150** may be electrically connected to the above device.

The oxide insulating film **104** can have a function of supplying oxygen to the oxide semiconductor layer **106** as well as a function of preventing diffusion of an impurity from the substrate **102**; thus, the oxide insulating film **104** is an insulating film containing oxygen. It is particularly preferable that the oxide insulating film **104** be an insulating film containing excess oxygen. An oxide insulating film containing excess oxygen refers to an oxide insulating film from which oxygen can be released by heat treatment or the like. The oxide insulating film containing excess oxygen is preferably a film in which the amount of released oxygen when converted into oxygen atoms is 1.0×10^{19} atoms/cm^3 or more in thermal desorption spectroscopy analysis. Further, excess oxygen refers to oxygen which can be transferred in the oxide semiconductor layer, silicon oxide, or silicon oxynitride by heat treatment, oxygen in excess of an intrinsic stoichiometric composition, or oxygen which can fill Vo (oxygen vacancy) caused by lack of oxygen. Oxygen released from the oxide insulating film **104** can be diffused to a channel formation region of the oxide semiconductor layer **106**, so that oxygen vacancies which might be formed in the oxide semiconductor layer can be filled with the oxygen. In this manner, stable electrical characteristics of the transistor can be achieved.

Since the oxide insulating film **104** is provided in contact with the oxide semiconductor layer **106**, oxygen can be directly diffused to the oxide semiconductor layer **106** from a lower side of the oxide semiconductor layer **106**. Moreover, since the oxide insulating film **104** is provided in contact with the gate insulating film **112**, oxygen can be diffused to the oxide semiconductor layer **106** from an upper side of the oxide semiconductor layer **106** through the gate insulating film **112**.

Further, oxygen is introduced into the gate insulating film **112** by an ion implantation method and diffused to the oxide semiconductor layer **106** to the gate insulating film **112**.

More specifically, oxygen released from the oxide insulating film **104** can enter the upper side region of the oxide semiconductor layer **106**, which serves as a channel, by being transferred from the outside of the second source electrode layer **110***a* (the left side in FIG. **1**B) and the outside of the second drain electrode layer **110***b* (the right side in FIG. **1**B) through the gate insulating film **112**. In other words, the gate insulating film **112** is partly in contact with the oxide insulating film **104** so as to cover the second source electrode layer **110***a* and the second drain electrode layer **110***b*.

Thus, the gate insulating film **112** is provided between the protective insulating film **116**, and the second source electrode layer **110***a* and the second drain electrode layer **110***b* so that oxygen released from the oxide insulating film **104** can be diffused to the channel formation region in the oxide semiconductor layer **106**. Accordingly, a material to which little oxygen is diffused or transferred is used for the second source electrode layer **110***a*, the second drain electrode layer **110***b*, and the protective insulating film **116**. In this manner, when oxygen is diffused to the oxide semiconductor layer through the gate insulating film, diffusion or transfer of oxygen to the source electrode layer and the drain electrode layer can be suppressed.

In a transistor having such a structure, excess oxygen can be supplied from the oxide insulating film **104** and the gate insulating film **112** to the channel formation region of the oxide semiconductor layer **106**, whereby the transistor including the oxide semiconductor layer **106** has normally-off characteristics with a positive threshold voltage. Thus, it is possible to provide a semiconductor device in which an increase in oxygen vacancies in the oxide semiconductor layer **106** is suppressed. Further, a highly reliable semiconductor device can be provided.

Note that in the case where the substrate **102** is a substrate where another device is formed, the oxide insulating film **104** also has a function as an interlayer insulating film. In that case, the oxide insulating film **104** is preferably subjected to planarization treatment such as chemical mechanical polishing (CMP) treatment so as to have a flat surface.

An oxide semiconductor that can be used for the oxide semiconductor layer **106** preferably contains at least indium (In) or zinc (Zn). Alternatively, the oxide semiconductor preferably contains both In and Zn. Details of a material and a formation method which can be used for the oxide semiconductor layer **106** are to be described in description of a method for manufacturing the transistor.

Note that stable electrical characteristics can be effectively imparted to a transistor in which an oxide semiconductor layer serves as a channel by reducing the concentration of impurities in the oxide semiconductor layer to make the oxide semiconductor layer intrinsic or substantially intrinsic. The term "substantially intrinsic" refers to the state where an oxide semiconductor layer has a carrier density lower than 1×10^{17}/cm^3, preferably lower than 1×10^{15}/cm^3, further preferably lower than 1×10^{13}/cm^3.

Further, in an oxide semiconductor layer, hydrogen, nitrogen, carbon, silicon, and metal elements except main components of the oxide semiconductor are impurities. For example, hydrogen and nitrogen form donor levels to increase the carrier density. Silicon forms impurity levels in an oxide semiconductor layer. The impurity levels serve as traps and might cause electrical characteristics of the transistor to deteriorate.

An oxide semiconductor layer can be intrinsic or substantially intrinsic under the following conditions: in SIMS analysis, the concentration of silicon is lower than 1×10^{19} atoms/cm^3, preferably lower than 5×10^{18} atoms/cm^3, further preferably lower than 1×10^{18} atoms/cm^3; the concentration of hydrogen is lower than or equal to 2×10^{20} atoms/cm^3, preferably lower than or equal to 5×10^{19} atoms/cm^3, further preferably lower than or equal to 1×10^{19} atoms/cm^3, still further preferably lower than or equal to 5×10^{18} atoms/cm^3; and the concentration of nitrogen is lower than 5×10^{19} atoms/cm^3, preferably lower than or equal to 5×10^{18} atoms/cm^3, further preferably lower than or equal to 1×10^{18} atoms/cm^3, still further preferably lower than or equal to 5×10^{17} atoms/cm^3.

In the case where the oxide semiconductor layer includes crystals, high concentration of silicon or carbon might reduce the crystallinity of the oxide semiconductor layer. The crystallinity of the oxide semiconductor layer can be prevented from decreasing when the concentration of silicon is lower than 1×10^{19} atoms/cm^3, preferably lower than 5×10^{18} atoms/cm^3, further preferably lower than 1×10^{18} atoms/cm^3, and the concentration of carbon is lower than 1×10^{19} atoms/cm^3, preferably lower than 5×10^{18} atoms/cm^3, further preferably lower than 1×10^{18} atoms/cm^3.

A transistor in which a highly purified oxide semiconductor film is used for a channel formation region as described above has extremely low off-state current, and the off-state current standardized on the channel width of the transistor can be as low as several yoktoamperes per micrometer to several zeptoamperes per micrometer.

When the density of localized states in the film of the oxide semiconductor which can be used for the oxide semiconductor layer **106** is reduced, stable electrical characteristics can be imparted to the transistor including the oxide semiconductor layer **106**. Note that to impart stable electrical characteristics to the transistor, the absorption coefficient due to the localized states in the oxide semiconductor layer **106**, which is obtained in measurement by a constant photocurrent method (CPM), is set lower than 1×10^{-3}/cm, preferably lower than 3×10^{-4}/cm.

For the first source electrode layer **108***a* and the first drain electrode layer **108***b*, a conductive material which is easily bonded to oxygen can be used. For example, Al, Cr, Cu, Ta, Ti, Mo, or W can be used. In particular, W with a high melting point is preferably used, which allows subsequent process temperatures to be relatively high. Note that the conductive material which is easily bonded to oxygen includes, in its category, a material to which oxygen is easily diffused or transferred.

When the conductive material which is easily bonded to oxygen is in contact with an oxide semiconductor layer, a phenomenon occurs in which oxygen of the oxide semiconductor layer is diffused or transferred to the conductive material which is easily bonded to oxygen. Since the manufacturing process of the transistor involves some heat treatment steps, the above phenomenon causes generation of oxygen vacancies in a region of the oxide semiconductor layer, which is in contact with the source electrode or the drain electrode, and the region becomes an n-type. Thus, the n-type region can serve as a source or a drain of the transistor.

However, in the case of forming a transistor with an extremely short channel length, the n-type region which is formed by the generation of the oxygen vacancies sometimes extends in the channel length direction of the transistor. In that case, electrical characteristics of the transistor change; for example, the threshold voltage is shifted or on and off of the transistor cannot be controlled with the gate voltage (i.e., the transistor is on). Accordingly, when a transistor with an extremely short channel length is formed, it is not preferable that the conductive material which is easily bonded to oxygen be used for a source electrode and a drain electrode.

Thus, in one embodiment of the present invention, the source electrode and the drain electrode have stacked-layer structures, and the second source electrode layer **110***a* and the second drain electrode layer **110***b*, which determine the channel length, are formed using the conductive material which is not easily bonded to oxygen. As the conductive material, for example, a conductive nitride such as tantalum nitride or titanium nitride, or ruthenium is preferably used. Note that the conductive material which is not easily bonded to oxygen includes, in its category, a material to which oxygen is not easily diffused or transferred.

Note that in the transistor having the structure illustrated in FIGS. **1**A to **1**E, the channel length refers to a distance between the second source electrode layer **110***a* and the second drain electrode layer **110***b*.

By the use of the above conductive material which is not easily bonded to oxygen for the second source electrode layer **110***a* and the second drain electrode layer **110***b*, generation of oxygen vacancies in the channel formation region of the oxide semiconductor layer **106** can be suppressed, so that change of the channel into an n-type can be suppressed. In this manner, even a transistor with an extremely short channel length can have favorable electrical characteristics.

In the case where the source electrode and the drain electrode are formed using only the above conductive material which is not easily bonded to oxygen, the contact resistance with the oxide semiconductor layer **106** becomes too high; thus, it is preferable that as illustrated in FIG. **1**B, the first source electrode layer **108***a* and the first drain electrode layer **108***b* be formed over the oxide semiconductor layer **106** and the second source electrode layer **110***a* and the second drain electrode layer **110***b* be formed so as to cover the first source electrode layer **108***a* and the first drain electrode layer **108***b*.

At this time, it is preferable that the oxide semiconductor layer **106** have a large contact area with the first source electrode layer **108***a* or the first drain electrode layer **108***b*, and the oxide semiconductor layer **106** have a small contact area with the second source electrode layer **110***a* or the second drain electrode layer **110***b*. The region of the oxide semiconductor layer **106**, which is in contact with the first source electrode layer **108***a* or the first drain electrode layer **108***b*, becomes an n-type region due to generation of oxygen vacancies. Owing to the n-type region, the contact resistance between the oxide semiconductor layer **106** and the first source electrode layer **108***a* or the first drain electrode layer **108***b* can be reduced. Accordingly, when the oxide semiconductor layer **106** has a large contact area with the first source electrode layer **108***a* or the first drain electrode layer **108***b*, the area of the n-type region can also be large.

Here, the above-mentioned n-type region is described with reference to FIG. **1**E. FIG. **1**E is an enlarged view of a region **105** illustrated in FIG. **1**B, and in the region of the oxide semiconductor layer **106**, which is in contact with the first source electrode layer **108***a*, oxygen of the oxide semiconductor layer **106** is extracted to the first source electrode layer **108***a* side, so that an n-type region **106***a* is formed. Note that the n-type region **106***a* is a region of the oxide semiconductor layer **106**, which includes many oxygen vacancies. Moreover, a component of the first source electrode layer **108***a*, for example, a tungsten element in the case where a tungsten film is used for the first source electrode layer **108***a*, enters the n-type region **106***a*. In addition, although not illustrated, a mixed layer might be formed due to entry of oxygen of the oxide semiconductor layer **106** into a region of the first source electrode layer **108***a*, which is in contact with the oxide semiconductor layer **106**.

Note that although the region **105** has been described with reference to the enlarged view illustrating the oxide semiconductor layer **106** and the first source electrode layer **108***a*, the above-described n-type region is also formed on the first drain electrode layer **108***b* side of the oxide semiconductor layer **106**.

Note that the n-type region **106***a* may be used as a source region or a drain region in the oxide semiconductor layer **106**.

Further, the conductive material which is not easily bonded to oxygen is used for the second source electrode layer **110***a* and the second drain electrode layer **110***b*. Thus, when the oxide semiconductor layer **106** is supplied with oxygen of the oxide insulating film **104** from the upper side of the oxide semiconductor layer **106** through the gate insulating film **112**, the oxygen is less likely to be diffused or transferred to the second source electrode layer **110***a* and the second drain electrode layer **110***b*. Accordingly, oxygen can be favorably supplied to the oxide semiconductor layer **106**.

The gate insulating film **112** can be formed using an insulating film containing one or more of aluminum oxide, magnesium oxide, silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, and tantalum oxide. The gate insulating film **112** may be a stack of any of the above materials.

For the gate electrode layer **114**, a conductive film including a material such as Al, Ti, Cr, Co, Ni, Cu, Y, Zr, Mo, Ru, Ag, Ta, or W can be used. Further, the gate electrode layer **114** may be a stack of any of the above materials.

It is preferable that a material to which little oxygen is diffused or transferred be used for the protective insulating film **116**. Further, a material containing little hydrogen when formed into a film is preferably used for the protective insulating film **116**. The hydrogen content of the protective insulating film **116** is preferably lower than $5\times10^{19}/cm^3$, further preferably lower than $5\times10^{18}/cm^3$. When the hydrogen content of the protective insulating film **116** has the above value, off-state current of the transistor can be low. For example, a silicon nitride film or a silicon nitride oxide film is preferably used as the protective insulating film **116**.

Here, distances between the components are described with reference to the cross-sectional view in FIG. **1**D.

The distance (L1) between the first source electrode layer **108***a* and the first drain electrode layer **108***b* is set to 0.8 μm or longer, preferably 1.0 μm or longer. In the case where L1 is shorter than 0.8 μm, influence of oxygen vacancies generated in the channel formation region cannot be eliminated, which might cause deterioration of the electrical characteristics of the transistor.

Even when the distance (L2) between the second source electrode layer **110***a* and the second drain electrode layer **110***b* is shorter than L1, for example, 30 nm or shorter, the transistor can have favorable electrical characteristics.

Further, when the width of the gate electrode layer **114** is referred to as L0, L0≥L1≥L2 (L1 is longer than or equal to L2 and shorter than or equal to L0) is satisfied as illustrated in FIG. **1**D so that regions can be formed in which the gate electrode layer **114** overlaps with the source and drain electrode layers (the first source electrode layer **108***a*, the second source electrode layer **110***a*, the first drain electrode layer **108***b*, and the second drain electrode layer **110***b*) with the gate insulating film **112** provided therebetween. With use of such a structure, on-state characteristics (e.g., on-state current and field-effect mobility) of a miniaturized transistor can be improved.

When the width of the oxide semiconductor layer **106** is referred to as L3 and the width of the transistor **150** is referred to as L4, L3 is preferably shorter than 1 μm and L4 is preferably longer than or equal to 1 μm and shorter than or equal to 2.5 μm. When L3 and L4 have the respective values, the transistor can be miniaturized.

The above is the transistor of one embodiment of the present invention, whose structure can suppress an increase in oxygen vacancies in the oxide semiconductor layer. Specifically, in the transistor, oxygen can be supplied from the oxide insulating film and the gate insulating film, which are in contact with the oxide semiconductor layer, to the oxide semiconductor layer. It is thus possible to provide a semiconductor device having favorable electrical characteristics and high long-term reliability.

Note that this embodiment can be combined as appropriate with any of the other embodiments and examples in this specification.

Embodiment 2

In this embodiment, a method for manufacturing the transistor **150** described in Embodiment 1 with reference to FIGS. **1**A to **1**E will be described with reference to FIGS. **2**A to **2**D, FIGS. **3**A to **3**D, and FIGS. **4**A to **4**C.

For the substrate **102**, a glass substrate, a ceramic substrate, a quartz substrate, a sapphire substrate, or the like can be used. Alternatively, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate made of silicon, silicon carbide, or the like, a compound semiconductor substrate made of silicon germanium or the like, a silicon-on-insulator (SOI) substrate, or the like may be used. Still alternatively, any of these substrates further provided with a semiconductor element may be used.

The oxide insulating film **104** can be formed by a plasma chemical vapor deposition (CVD) method, a sputtering method, or the like using an oxide insulating film of aluminum oxide, magnesium oxide, silicon oxide, silicon oxynitride, silicon nitride oxide, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, tantalum oxide, or the like or a mixed material of any of these. Further, a stack of any of the above materials may be used, and at least an upper layer of the oxide insulating film **104**, which is in contact with the oxide semiconductor layer **106**, is formed using a material containing oxygen which might serve as a supply source of oxygen to the oxide semiconductor layer **106**.

Oxygen may be added to the oxide insulating film **104** by an ion implantation method, an ion doping method, a plasma immersion ion implantation method, or the like. By addition of oxygen, the oxide insulating film **104** can further contain excess oxygen.

Then, an oxide semiconductor layer is formed over the oxide insulating film **104** by a sputtering method, a CVD method, a molecular beam epitaxy (MBE) method, an atomic layer deposition (ALD) method, or a pulse laser deposition (PLD) method and selectively etched, so that the oxide semiconductor layer **106** is formed (see FIG. **2**A). Note that heating may be performed before etching.

An oxide semiconductor that can be used for the oxide semiconductor layer **106** preferably contains at least indium (In) or zinc (Zn). Alternatively, the oxide semiconductor preferably contains both In and Zn. In order to reduce fluctuations in electrical characteristics of the transistors including the oxide semiconductor, the oxide semiconductor preferably contains a stabilizer in addition to In and Zn.

As a stabilizer, gallium (Ga), tin (Sn), hafnium (Hf), aluminum (Al), zirconium (Zr), and the like can be given. As another stabilizer, lanthanoid such as lanthanum (La), cerium (Ce), praseodymium (Pr), neodymium (Nd), samarium (Sm), europium (Eu), gadolinium (Gd), terbium (Tb), dysprosium (Dy), holmium (Ho), erbium (Er), thulium (Tm), ytterbium (Yb), or lutetium (Lu) can be given.

As the oxide semiconductor, for example, any of the following can be used: indium oxide, tin oxide, zinc oxide, an In—Zn oxide, a Sn—Zn oxide, an Al—Zn oxide, a Zn—Mg oxide, a Sn—Mg oxide, an In—Mg oxide, an In—Ga oxide, an In—Ga—Zn oxide, an In—Al—Zn oxide, an In—Sn—Zn oxide, a Sn—Ga—Zn oxide, an Al—Ga—Zn oxide, a Sn—Al—Zn oxide, an In—Hf—Zn oxide, an In—La—Zn oxide, an In—Ce—Zn oxide, an In—Pr—Zn oxide, an In—Nd—Zn oxide, an In—Sm—Zn oxide, an In—Eu—Zn oxide, an In—Gd—Zn oxide, an In—Tb—Zn oxide, an In—Dy—Zn oxide, an In—Ho—Zn oxide, an In—Er—Zn oxide, an In—Tm—Zn oxide, an In—Yb—Zn oxide, an In—Lu—Zn oxide, an In—Sn—Ga—Zn oxide, an In—Hf—Ga—Zn oxide, an In—Al—Ga—Zn oxide, an In—Sn—Al—Zn oxide, an In—Sn—Hf—Zn oxide, or an In—Hf—Al—Zn oxide.

Note that an In—Ga—Zn oxide refers to, for example, an oxide containing In, Ga, and Zn as its main components and there is no particular limitation on the ratio of In to Ga and Zn. The In—Ga—Zn oxide may contain a metal element other than In, Ga, and Zn. Further, in this specification, a film formed using an In—Ga—Zn oxide is also referred to as an IGZO film.

Alternatively, a material represented by $InMO_3(ZnO)_m$ (m>0, where m is not an integer) may be used. Note that M represents one or more metal elements selected from Ga, Fe, Mn, and Co. Further alternatively, a material represented by $In_2SnO_5(ZnO)_n$ (n>0, where n is an integer) may be used.

Note that the oxide semiconductor film is preferably formed by a sputtering method. As a sputtering method, an RF sputtering method, a DC sputtering method, an AC sputtering method, or the like can be used. In particular, a DC sputtering method is preferably used because dust generated in the deposition can be reduced and the film thickness can be uniform.

As the oxide semiconductor film, a film in a single crystal state, a polycrystalline (also referred to as polycrystal) state, an amorphous state, or the like can be used. The oxide semiconductor film is preferably a c-axis aligned crystalline oxide semiconductor (CAAC-OS) film.

Sputtering may be performed to form an oxide semiconductor film including a CAAC-OS film. In order to obtain a CAAC-OS film by sputtering, it is important to form crystals in a hexagonal configuration in an initial stage of deposition of an oxide semiconductor film and to cause crystal growth from the crystals as cores. In order to achieve this, it is preferable that the distance between the target and the substrate be made to be longer (e.g., 150 mm to 200 mm) and a substrate heating temperature be 100° C. to 500° C., more preferably 200° C. to 400° C., still preferably 250° C. to 300° C. In addition to this, the deposited oxide semiconductor film is subjected to heat treatment at a temperature higher than the substrate heating temperature in the deposition. Therefore, micro-defects in the film and defects at the interface of a stacked layer can be compensated.

The CAAC-OS film is one of oxide semiconductor films having a plurality of c-axis aligned crystal parts. In a transmission electron microscope (TEM) image of the CAAC-OS film, a boundary between crystal parts, that is, a grain boundary is not clearly observed. Thus, in the CAAC-OS film, a reduction in electron mobility due to the grain boundary is less likely to occur. According to the TEM image of the CAAC-OS film observed in a direction substantially parallel to a sample surface (cross-sectional TEM image), metal atoms are arranged in a layered manner in the crystal parts. Each metal atom layer has a morphology reflected by a surface over which the CAAC-OS film is formed (hereinafter, a surface over which the CAAC-OS film is formed is referred to as a formation surface) or a top surface of the CAAC-OS film, and is arranged in parallel to the formation surface or the top surface of the CAAC-OS film. On the other hand, according to the TEM image of the CAAC-OS film observed in a direction substantially perpendicular to the sample surface (plan TEM image), metal atoms are arranged in a triangular or hexagonal configuration in the crystal parts. However, there is no regularity of arrangement of metal atoms between different crystal parts.

In each of the crystal parts included in the CAAC-OS film, a c-axis is aligned in a direction parallel to a normal vector of a surface where the CAAC-OS film is formed or a normal vector of a surface of the CAAC-OS film, triangular or hexagonal atomic arrangement which is seen from the direction perpendicular to the a-b plane is formed, and metal atoms are arranged in a layered manner or metal atoms and oxygen atoms are arranged in a layered manner when seen from the direction perpendicular to the c-axis. Note that, among crystal parts, the directions of the a-axis and the b-axis of one crystal part may be different from those of another crystal part. In this specification, a simple term "perpendicular" includes a range from 85° to 95°. In addition, a simple term "parallel" includes a range from −5° to 5°.

In the CAAC-OS film, distribution of c-axis aligned crystal parts is not necessarily uniform. For example, in the case where crystal growth leading to the crystal parts of the CAAC-OS film occurs from the vicinity of the top surface of the film, the proportion of the c-axis aligned crystal parts in the vicinity of the top surface is higher than that in the vicinity of the formation surface in some cases. Further, when an impurity is added to the CAAC-OS film, a region to which the impurity is added is altered, and the proportion of the c-axis aligned crystal parts in the CAAC-OS film varies depending on regions, in some cases.

Since the c-axes of the crystal parts included in the CAAC-OS film are aligned in the direction parallel to a normal vector of a surface where the CAAC-OS film is formed or a normal vector of a surface of the CAAC-OS film, the directions of the c-axes may be different from each other depending on the shape of the CAAC-OS film (the cross-sectional shape of the surface where the CAAC-OS film is formed or the cross-sectional shape of the surface of the CAAC-OS film). Note that when the CAAC-OS film is formed, the direction of c-axis of the crystal part is the direction parallel to a normal vector of the surface where the CAAC-OS film is formed or a normal vector of the surface of the CAAC-OS film. The crystal part is formed by film formation or by performing treatment for crystallization such as heat treatment after film formation.

With use of the CAAC-OS film in a transistor, change in electric characteristics of the transistor due to irradiation with visible light or ultraviolet light is small. Thus, the transistor has high reliability.

For example, a CAAC-OS film can be deposited by a sputtering method using a polycrystalline oxide semiconductor sputtering target. When ions collide with the sputtering target, a crystal region included in the sputtering target might be separated from the target along an a-b plane; in other words, a sputtered particle having a plane parallel to an a-b plane (flat-plate-like sputtered particle or pellet-like sputtered particle) might be separated from the sputtering target. In that case, the flat-plate-like sputtered particle reaches a substrate while maintaining their crystal state, whereby the CAAC-OS film can be formed.

For the deposition of the CAAC-OS film, the following conditions are preferably used.

By reducing the amount of impurities entering the CAAC-OS film during the deposition, the crystal state can be prevented from being distorted by the impurities. For example, impurities (e.g., hydrogen, water, carbon dioxide, or nitrogen) which exist in the deposition chamber may be reduced. Furthermore, impurities in a deposition gas may be reduced. Specifically, a deposition gas whose dew point is −80° C. or lower, preferably −100° C. or lower is used.

By increasing the substrate heating temperature during the deposition, migration of a sputtered particle is likely to occur after the sputtered particle reaches a substrate surface. Specifically, the substrate heating temperature during the deposition is higher than or equal to 100° C. and lower than or equal to 740° C., preferably higher than or equal to 200° C. and lower than or equal to 500° C. By increasing the substrate heating temperature during the deposition, when the flat-plate-like sputtered particle reaches the substrate, migration occurs on the substrate surface, so that a flat plane of the flat-plate-like sputtered particle is attached to the substrate.

Furthermore, it is preferable that the proportion of oxygen in the deposition gas be increased and the power be optimized in order to reduce plasma damage at the deposition. The proportion of oxygen in the deposition gas is 30 vol % or higher, preferably 100 vol %.

As an example of the sputtering target, an In—Ga—Zn—O compound target is described below.

The In—Ga—Zn—O compound target, which is polycrystalline, is made by mixing InO_X powder, GaO_Y powder, and ZnO_Z powder in a predetermined molar ratio, applying pressure, and performing heat treatment at a temperature higher than or equal to 1000° C. and lower than or equal to 1500° C. Note that X, Y, and Z are each a given positive number. The kinds of powder and the molar ratio for mixing powder may be determined as appropriate depending on the sputtering target that is formed.

Next, first heat treatment is preferably performed. The first heat treatment may be performed at a temperature higher than or equal to 250° C. and lower than or equal to 650° C., preferably higher than or equal to 300° C. and lower than or equal to 500° C., in an inert gas atmosphere, an atmosphere containing an oxidizing gas at 10 ppm or more, or a reduced pressure state. Alternatively, the first heat treatment may be performed in such a manner that heat treatment is performed in an inert gas atmosphere, and then another heat treatment is performed in an atmosphere containing an oxidizing gas at 10 ppm or more in order to compensate released oxygen. By the first heat treatment, the crystallinity of the oxide semiconductor layer **106** can be improved, and in addition, impurities such as hydrogen and water can be removed from the oxide insulating film **104** and the oxide semiconductor layer **106**. Note that the step of the first heat treatment may be performed before etching for formation of the oxide semiconductor layer **106**.

Then, a first conductive film **108** to be the first source electrode layer **108***a* and the first drain electrode layer **108***b* is formed over the oxide semiconductor layer **106** (see FIG. **2**B). For the first conductive film **108**, Al, Cr, Cu, Ta, Ti, Mo, W, or an alloy material containing any of these as a main component can be used. For example, a 100-nm-thick tungsten film is formed by a sputtering method or the like.

Next, resist masks **190***a* and **190***b* are formed over the first conductive film **108** (see FIG. **2**C).

After that, the first conductive film **108** is etched so as to be divided over the oxide semiconductor layer **106** with use of the resist masks **190***a* and **190***b* as masks, so that the first source electrode layer **108***a* and the first drain electrode layer **108***b* are formed; then, the resist masks **190***a* and **190***b* are removed (see FIG. **2**D).

At this time, the first conductive film **108** is over-etched, so that the oxide semiconductor layer **106** is partly etched as illustrated in FIG. **2**D. However, when the etching selectivity of the first conductive film **108** to the oxide semiconductor layer **106** is high, the oxide semiconductor layer **106** is hardly etched.

In addition, by over-etching the first conductive film **108**, part of the oxide insulating film **104**, more specifically, the oxide insulating film **104** on outer sides than the edges of the first source electrode layer **108***a* and the first drain electrode layer **108***b* is etched as illustrated in FIG. **2**D.

Then, a second conductive film **110** that is to be the second source electrode layer **110***a* and the second drain electrode layer **110***b* is formed over the oxide semiconductor layer **106**, the first source electrode layer **108***a*, and the first drain electrode layer **108***b* (see FIG. **3**A). For the second conductive film **110**, a conductive nitride such as tantalum nitride or titanium nitride, ruthenium, or an alloy material containing any of these as a main component can be used. For example, a 20-nm-thick tantalum nitride film is formed by a sputtering method or the like.

Next, the second conductive film **110** is etched so as to be divided, so that the second source electrode layer **110***a* and the second drain electrode layer **110***b* are formed (see FIG. **3**B). At this time, as illustrated in FIG. **3**B, part of the oxide semiconductor layer **106** may be etched. Although not illustrated, at the time of etching for formation of the second source electrode layer **110***a* and the second drain electrode layer **110***b*, part of the oxide insulating film **104**, more specifically, the oxide insulating film **104** on outer sides than the edges of the second source electrode layer **110***a* and the second drain electrode layer **110***b* may be etched.

Note that in the case of forming a transistor whose channel length (a distance between the second source electrode layer **110***a* and the second drain electrode layer **110***b*) is extremely short, the second source electrode layer **110***a* and the second drain electrode layer **110***b* can be formed in such a manner that the second conductive film **110** is etched first so as to cover the first source electrode layer **108***a* and the first drain electrode layer **108***b*, and then etched using resist masks that are processed by a method suitable for fine line processing, such as electron beam exposure. Note that by use of a positive type resist for the resist masks, the exposed region can be minimized and throughput can be thus improved. In the above manner, a transistor having a channel length of 30 nm or less can be formed.

Next, second heat treatment is preferably performed. The second heat treatment can be performed under a condition similar to that of the first heat treatment. By the second heat treatment, impurities such as hydrogen and water can be further removed from the oxide semiconductor layer **106**.

Next, the gate insulating film **112** is formed over the oxide insulating film **104**, the oxide semiconductor layer **106**, the second source electrode layer **110***a*, and the second drain electrode layer **110***b*. The gate insulating film **112** can be formed using aluminum oxide, magnesium oxide, silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, tantalum oxide, or the like. The gate insulating film **112** may be a stack of any of the above materials. The gate insulating film **112** can be formed by a sputtering method, a CVD method, an MBE method, an ALD method, a PLD method, or the like.

It is preferable that the gate insulating film **112** be successively subjected to heat treatment after being formed. For example, the gate insulating film **112** is formed with a PE-CVD apparatus and is successively subjected to heat treatment in a vacuum. The heat treatment can remove hydrogen, moisture, and the like from the gate insulating film **112**. By the heat treatment, the gate insulating film **112** can be dehydrated or dehydrogenated to be dense.

After the heat treatment, oxygen is added into the gate insulating film **112** by an ion implantation method, an ion doping method, a plasma immersion ion implantation method, or the like (see FIG. **3**C). By addition of oxygen, the gate insulating film **112** can contain excess oxygen. FIG. **3**C is a schematic view which illustrates addition of oxygen **120** into the gate insulating film **112**. The oxygen **120** contains at least any of an oxygen radical, ozone, an oxygen atom, and an oxygen ion (including an oxygen molecular ion or an oxygen cluster ion). Note that there is not particular restriction of a timing of the step of adding oxygen into the gate insulating film **112** as long as the step is performed after the formation of the gate insulating film **112**, and the step may be performed after formation of a gate electrode or after formation of a protective insulating film.

Next, a third conductive film **113** that is to be the gate electrode layer **114** is formed over the gate insulating film **112**, and then a resist mask **192** is formed in a desired region (see FIG. **3**D). For the third conductive film **113**, Al, Ti, Cr, Co, Ni, Cu, Y, Zr, Mo, Ru, Ag, Ta, W, or an alloy material containing any of these as a main component can be used. The third conductive film **113** can be formed by a sputtering method.

Then, the third conductive film **113** is etched, so that the gate electrode layer **114** is formed; then, the resist mask **192** is removed (see FIG. **4**A).

Next, the protective insulating film **116** is formed over the gate insulating film **112** and the gate electrode layer **114**. It is preferable that a material to which little oxygen is diffused or transferred be used for the protective insulating film **116**. Further, a material containing little hydrogen when formed into a film is preferably used for the protective insulating film **116**. The hydrogen content of the protective insulating film **116** is preferably lower than $5\times10^{19}/cm^3$, further preferably lower than $5\times10^{18}/cm^3$. When the hydrogen content of the protective insulating film **116** has the above value, off-state current of the transistor can be low.

For example, a silicon nitride film or a silicon nitride oxide film is preferably used as the protective insulating film **116**. The protective insulating film **116** can be formed by a sputtering method, a CVD method, an MBE method, an ALD method, or a PLD method. In particular, for the protective insulating film **116**, a silicon nitride film is preferably formed by a sputtering method, in which case the content of water or hydrogen is low.

After the protective insulating film **116** is formed, the oxygen **120** is added to the gate insulating film **112** by an ion implantation method, an ion doping method, a plasma immersion ion implantation method, or the like (see FIG. **4**B). Addition of the oxygen in this step is performed through the protective insulating film **116**. Further, the number of times of the step of adding oxygen is not particularly limited as long as the step is performed after formation of the gate insulating film **112**, and the step may be performed after formation of the gate electrode layer **114**, and further performed after formation of the protective insulating film **116**.

Further, addition of oxygen is not necessarily performed twice (one is performed after the formation of the gate insulating film **112** and the other is performed after formation of the protective insulating film **116**), and either one of the steps may be performed.

Oxygen may be added to the entire surface of the substrate at a time. Alternatively, a linear ion beam may be used, for example. In the case of using the linear ion beam, the substrate or the ion beam is relatively moved (scanned), whereby the oxygen **120** can be introduced into the entire area of the gate insulating film **112**.

As a supply gas of the oxygen **120**, a gas containing oxygen (O) can be used; for example, an O_2 gas, an N_2O gas, a CO_2 gas, a CO gas, or an NO_2 gas can be used. Note that a rare gas (e.g., an Ar gas) may be contained in the supply gas of the oxygen.

In the case where oxygen is added by, for example, an ion implantation method, the dose of the oxygen **120** is preferably greater than or equal to 1×10^{13} ions/cm^2 and less than or equal to 5×10^{16} ions/cm^2. For example, in the case where silicon oxide whose composition is represented by SiO_x ($x>0$) is used, since a single crystal of silicon oxide is SiO_2, x in the insulating film containing excess oxygen is preferably greater than 2. Note that such a region containing oxygen in excess of the stoichiometric composition may exist in part of the gate insulating film **112**. The depth at which oxygen is introduced may be adjusted as appropriate by implantation conditions.

Next, third heat treatment is preferably performed. The third heat treatment can be performed under a condition similar to that of the first heat treatment. By the third heat treatment, oxygen is easily released from the oxide insulating film **104** and the gate insulating film **112**, so that oxygen vacancies in the oxide semiconductor layer **106** can be reduced.

Through the above steps, the transistor **150** illustrated in FIGS. **1**A to **1**E and FIG. **4**C can be manufactured.

Note that this embodiment can be combined as appropriate with any of the other embodiments and examples in this specification.

Embodiment 3

In this embodiment, a transistor having a structure different from that of the transistor described in Embodiment 1 will be described with reference to FIGS. **5**A to **5**C and FIGS. **6**A to **6**D.

FIGS. **5**A, **5**B, and **5**C are a top view and cross-sectional views which illustrate a transistor of one embodiment of the present invention. FIG. **5**A is the top view of the transistor, and a cross section taken along a dashed-dotted line X**2**-Y**2** in FIG. **5**A is illustrated in FIG. **5**B. A cross section taken along a dashed-dotted line V**2**-W**2** in FIG. **5**A is illustrated in FIG. **5**C. Note that for simplification of the drawing, some components in the top view in FIG. **5**A are illustrated in a see-through manner or not illustrated. Note that the same portions as or portions having functions similar to those of the transistor described in Embodiment 1 are denoted by the same reference numerals, and repeated description thereof is omitted.

A transistor **152** illustrated in FIGS. **5**A, **5**B, and **5**C includes the oxide insulating film **104** formed over the substrate **102**; the oxide semiconductor layer **106** formed over the oxide insulating film **104**; a first source electrode layer **168*a*** and a first drain electrode layer **168*b*** formed over the oxide semiconductor layer **106**; the second source electrode layer **110*a*** and the second drain electrode layer **110*b*** formed over the first source electrode layer **168*a*** and the first drain electrode layer **168*b***, respectively; the gate insulating film **112** formed over the oxide insulating film **104**, the oxide semiconductor layer **106**, the second source electrode layer **110*a***, and the second drain electrode layer **110*b***; the gate electrode layer **114** formed over the gate insulating film **112** and in a position overlapping with the oxide semiconductor layer **106**; and the protective insulating film **116** formed over the gate insulating film **112** and the gate electrode layer **114**. Note that another insulating layer, another wiring, or the like may be formed over the protective insulating film **116**.

The transistor **152** described in this embodiment is different from the transistor **150** described in Embodiment 1 in the shapes of the first source electrode layer **168*a*** and the first drain electrode layer **168*b***. Note that the second source electrode layer **110*a***, the second drain electrode layer **110*b***, the gate insulating film **112**, the gate electrode layer **114**, and the protective insulating film **116** which are formed over the first source electrode layer **168*a*** and the first drain electrode layer **168*b*** have shapes corresponding to the shapes of the first source electrode layer **168*a*** and the first drain electrode layer **168*b***.

With the staircase-like shapes of the first source electrode layer **168*a*** and the first drain electrode layer **168*b*** as illustrated in FIG. **5**B, the second source electrode layer **110***a*, the second drain electrode layer **110***b*, and the gate insulating film **112** can have favorable coverage. When the gate insulating film **112** has favorable coverage, oxygen released from the oxide insulating film **104** is likely to be diffused to an upper region of the oxide semiconductor layer **106**, which serves as a channel, through the gate insulating film **112**.

Here, a method for manufacturing the transistor **152** will be described with reference to FIGS. **6**A to **6**D.

In the manufacturing process of the transistor **152**, steps before FIG. **6**A are performed in a manner similar to those up to FIG. **2**C in the manufacturing process of the transistor **150** (see FIG. **6**A). Note that the cross-sectional structure illustrated in FIG. **6**A is the same as that illustrated in FIG. **2**C.

Next, the first conductive film **108** is etched using the resist masks **190***a* and **190***b* to form the first source electrode layer **108***a* and the first drain electrode layer **108***b* (see FIG. **6**B).

Next, resist masks **194***a* and **194***b* are formed by making the resist masks **190***a* and **190***b* recede or reducing them by ashing (see FIG. **6**C).

Next, the first source electrode layer **108***a* and the first drain electrode layer **108***b* are etched using the resist masks **194***a* and **194***b* and then the resist masks **194***a* and **194***b* are removed, whereby the first source electrode layer **168***a* and the first drain electrode layer **168***b* are formed (see FIG. **6**D).

By alternately performing plural times an etching step and a step of making the resist masks recede or reducing them by ashing, the end portions of the first source electrode layer **168***a* and the first drain electrode layer **168***b* can have staircase-like shapes.

Note that the subsequent steps are performed in manners similar to those of the corresponding steps in the manufacturing process of the transistor **150** described in the above embodiment, whereby the transistor **152** described in this embodiment can be fabricated.

The above is the transistor of one embodiment of the present invention, whose structure can suppress an increase in oxygen vacancies in the oxide semiconductor layer. Specifically, in the transistor, oxygen can be supplied from the oxide insulating film and the gate insulating film which are in contact with the oxide semiconductor layer to the oxide semiconductor layer. It is thus possible to provide a semiconductor device having favorable electrical characteristics and high long-term reliability.

Note that this embodiment can be combined as appropriate with any of the other embodiments and examples in this specification.

Embodiment 4

In this embodiment, a transistor having a structure different from that of the transistor described in Embodiment 1 will be described with reference to FIGS. **7**A to **7**D and FIGS. **8**A and **8**B.

FIGS. **7**A, **7**B, **7**C, and **7**D are a top view and cross-sectional views which illustrate a transistor of one embodiment of the present invention. FIG. **7**A is the top view of the transistor, and a cross section taken along a dashed-dotted line **X3**-**Y3** in FIG. **7**A is illustrated in FIG. **7**B. A cross section taken along a dashed-dotted line **V3**-**W3** in FIG. **7**A is illustrated in FIG. **7**C. FIG. **7**D illustrates widths of components of the transistor which are illustrated in FIG. **7**B. Note that for simplification of the drawing, some components in the top view in FIG. **7**A are illustrated in a see-through manner or not illustrated. Note that the same portions as or portions having functions similar to those of the transistor described in Embodiment 1 are denoted by the same reference numerals, and repeated description thereof is omitted.

A transistor **154** illustrated in FIGS. **7**A, **7**B, **7**C, and **7**D includes the oxide insulating film **104** formed over the substrate **102**; the oxide semiconductor layer **106** formed over the oxide insulating film **104**; the first source electrode layer **108***a* and the first drain electrode layer **108***b* formed over the oxide semiconductor layer **106**; the second source electrode layer **110***a* and the second drain electrode layer **110***b* formed over the first source electrode layer **108***a* and the first drain electrode layer **108***b*, respectively; the gate insulating film **112** formed over the oxide insulating film **104**, the oxide semiconductor layer **106**, the second source electrode layer **110***a*, and the second drain electrode layer **110***b*; a gate electrode layer **174** formed over the gate insulating film **112** and in a position overlapping with the oxide semiconductor layer **106**; and the protective insulating film **116** formed over the gate insulating film **112** and the gate electrode layer **174**. Note that another insulating layer, another wiring, or the like may be formed over the protective insulating film **116**.

The transistor **154** described in this embodiment is different from the transistor **150** described in Embodiment 1 in the shape of the gate electrode layer **174**. In the transistor **150**, the gate electrode layer **114** is provided in a position overlapping with the first source electrode layer **108***a*, the first drain electrode layer **108***b*, the second source electrode layer **110***a*, and the second drain electrode layer **110***b*; however, in the transistor **154** described in this embodiment, the gate electrode layer **174** is provided in a position overlapping with the second source electrode layer **110***a* and the second drain electrode layer **110***b*. In other words, the gate electrode layer **174** is not provided in a position overlapping with the first source electrode layer **108***a* and the first drain electrode layer **108***b*.

Here, distances between the components are described with reference to the cross-sectional view in FIG. **7**D.

The distance (L1) between the first source electrode layer **108***a* and the first drain electrode layer **108***b* is set to 0.8 μm or longer, preferably 1.0 μm or longer. In the case where L1 is shorter than 0.8 μm, influence of oxygen vacancies generated in the channel formation region cannot be eliminated, which might cause deterioration of the electrical characteristics of the transistor.

Even when the distance (L2) between the second source electrode layer **110***a* and the second drain electrode layer **110***b* is shorter than L1, for example, 30 nm or shorter, the transistor can have favorable electrical characteristics.

When the width of the gate electrode layer **174** is referred to as L0, L1≥L0≥L2 (L0 is longer than or equal to L2 and shorter than or equal to L1) is satisfied so that parasitic capacitance which is caused between the gate and the drain and between the gate and the source can be made small as much as possible. Accordingly, the frequency characteristics of the transistor can be improved. Note that in order to obtain favorable electrical characteristics of the transistor, it is preferable that a difference between L0 and L2 be greater than or equal to 2 nm and less than or equal to 20 nm and a difference between L1 and L2 be greater than or equal to 20 nm and less than or equal to 1 μm.

Note that in a transistor that does not require high frequency characteristics, L0≥L1≥L2 (L1 is longer than or equal to L2 and shorter than or equal to L0) may be satisfied as illustrated in FIG. **1**B. With such a structure, the degree of difficulty in formation steps of the gate electrode can be lowered.

When the width of the oxide semiconductor layer **106** is referred to as L3 and the width of the transistor **154** is referred to as L4, L3 is preferably shorter than 1 μm and L4 is preferably longer than or equal to 1 μm and shorter than or equal to 2.5 μm. When L3 and L4 have the respective values, the transistor can be miniaturized.

Here, a manufacturing method of the transistor **154** will be described with reference to FIGS. **8**A and **8**B.

In a manufacturing process of the transistor **154**, steps before FIG. **8**A are performed in a manner similar to those up to FIG. **3**D in the manufacturing process of the transistor **150** (see FIG. **8**A). Note that the cross section illustrated in FIG. **8**A is different from the cross section illustrated in FIG. **3**D in the shape of a resist mask **196**.

Note that as the resist mask **196**, a mask having a finer pattern which is formed by performing a slimming process on a mask formed by a photolithography method or the like is preferably used. As the slimming process, an ashing process in which oxygen in a radical state (an oxygen radical) is used can be employed, for example. As a result of the slimming process, the line width of the mask formed by a photolithography method or the like can be reduced to a length shorter than or equal to the resolution limit of a light exposure apparatus, preferably less than or equal to half of the resolution limit of a light exposure apparatus, further preferably less than or equal to one third of the resolution limit of the light exposure apparatus. For example, the line width can be greater than or equal to 20 nm and less than or equal to 2000 nm, preferably greater than or equal to 50 nm and less than or equal to 350 nm.

Then, the third conductive film **113** is etched with use of the resist mask **196**, so that the gate electrode layer **174** is formed (see FIG. **8**B).

Note that the subsequent steps are performed in manners similar to those of the corresponding steps in the manufacturing process of the transistor **150** described in the above embodiment, whereby the transistor **154** described in this embodiment can be manufactured.

The above is the transistor of one embodiment of the present invention, whose structure can suppress an increase in oxygen vacancies in the oxide semiconductor layer. Specifically, in the transistor, oxygen can be supplied from the oxide insulating film and the gate insulating film which are in contact with the oxide semiconductor layer to the oxide semiconductor layer. It is thus possible to provide a semiconductor device having favorable electrical characteristics and high long-term reliability.

Note that this embodiment can be combined as appropriate with any of the other embodiments and examples in this specification.

Embodiment 5

In this embodiment, a transistor having a structure different from that of the transistor described in Embodiment 1 will be described with reference to FIGS. **9**A to **9**C and FIGS. **10**A to **10**C.

First, a transistor **156** illustrated in FIGS. **9**A to **9**C is described.

FIGS. **9**A, **9**B, and **9**C are a top view and cross-sectional views which illustrate a transistor of one embodiment of the present invention. FIG. **9**A is the top view of the transistor, and a cross section taken along a dashed-dotted line X**4**-Y**4** in FIG. **9**A is illustrated in FIG. **9**B. A cross section taken along a dashed-dotted line V**4**-W**4** in FIG. **9**A is illustrated in FIG. **9**C. Note that for simplification of the drawing, some components in the top view in FIG. **9**A are illustrated in a see-through manner or not illustrated. Note that the same portions as or portions having functions similar to those of the transistor described in Embodiment 1 are denoted by the same reference numerals, and repeated description thereof is omitted.

The transistor **156** illustrated in FIGS. **9**A, **9**B, and **9**C includes the oxide insulating film **104** formed over the substrate **102**; the oxide semiconductor layer **106** formed over the oxide insulating film **104**; the first source electrode layer **168*a*** and the first drain electrode layer **168*b*** formed over the oxide semiconductor layer **106**; the second source electrode layer **110*a*** and the second drain electrode layer **110*b*** formed over the first source electrode layer **168*a*** and the first drain electrode layer **168*b***, respectively; the gate insulating film **112** formed over the oxide insulating film **104**, the oxide semiconductor layer **106**, the second source electrode layer **110*a***, and the second drain electrode layer **110*b***; the gate electrode layer **174** formed over the gate insulating film **112** and in a position overlapping with the oxide semiconductor layer **106**; and the protective insulating film **116** formed over the gate insulating film **112** and the gate electrode layer **174**. Note that another insulating layer, another wiring, or the like may be formed over the protective insulating film **116**.

The transistor **156** described in this embodiment is different from the transistor **150** described in Embodiment 1 in the shapes of the first source electrode layer **168*a***, the first drain electrode layer **168*b***, and the gate electrode layer **174**. Note that the second source electrode layer **110*a***, the second drain electrode layer **110*b***, the gate insulating film **112**, the gate electrode layer **174**, and the protective insulating film **116** which are formed over the first source electrode layer **168*a*** and the first drain electrode layer **168*b*** have shapes corresponding to the shapes of the first source electrode layer **168*a*** and the first drain electrode layer **168*b***.

In the transistor **150**, the gate electrode layer **114** is provided in a position overlapping with the first source electrode layer **108*a***, the first drain electrode layer **108*b***, the second source electrode layer **110*a***, and the second drain electrode layer **110*b***; however, in the transistor **156** described in this embodiment, the gate electrode layer **174** is provided in a position overlapping with the second source electrode layer **110*a*** and the second drain electrode layer **110*b***. In other words, the gate electrode layer **174** is not provided in a position overlapping with the first source electrode layer **168*a*** and the first drain electrode layer **168*b***.

The transistor **156** described in this embodiment can be formed by referring to the manufacturing methods of the transistors **152** and **154** described in the above embodiments for the structures of the other components.

Next, a transistor **158** illustrated in FIGS. **10**A to **10**C is described.

The transistor **158** illustrated in FIGS. **10**A, **10**B, and **10**C includes the oxide insulating film **104** formed over the substrate **102**; the oxide semiconductor layer **106** formed over the oxide insulating film **104**; a first source electrode layer **178*a*** and a first drain electrode layer **178*b*** formed over the oxide semiconductor layer **106**; a second source electrode layer **180*a*** and a second drain electrode layer **180*b*** formed over the first source electrode layer **178*a*** and the first drain electrode layer **178*b***, respectively; the gate insulating film **112** formed over the oxide insulating film **104**, the oxide semiconductor layer **106**, the second source electrode layer **180*a***, and the second drain electrode layer **180*b***; the gate electrode layer **174** formed over the gate insulating film **112** and in a position overlapping with the oxide semiconductor layer **106**; and the protective insulating film **116** formed over the gate insulating film **112** and the gate electrode layer **174**. Note that another insulating layer, another wiring, or the like may be formed over the protective insulating film **116**.

The transistor **158** described in this embodiment is different from the transistor **150** described in Embodiment 1 in the shapes of the first source electrode layer **178***a*, the first drain electrode layer **178***b*, the second source electrode layer **180***a*, the second drain electrode layer **180***b*, and the gate electrode layer **174**. Note that the second source electrode layer **180***a*, the second drain electrode layer **180***b*, the gate insulating film **112**, the gate electrode layer **174**, and the protective insulating film **116** which are formed over the first source electrode layer **178***a* and the first drain electrode layer **178***b* have shapes corresponding to the shapes of the first source electrode layer **178***a* and the first drain electrode layer **178***b*.

With the shapes of the first source electrode layer **178***a* and the first drain electrode layer **178***b* as illustrated in FIG. **10**B, the second source electrode layer **180***a*, the second drain electrode layer **180***b*, and the gate insulating film **112** can have favorable coverage.

Further, the second source electrode layer **180***a* and the second drain electrode layer **180***b* are provided on inner sides than the edges of the first source electrode layer **178***a* and the first drain electrode layer **178***b* in the cross section in the channel length direction (FIG. **10**B). The first source electrode layer **178***a* and the first drain electrode layer **178***b* are not necessarily covered with the second source electrode layer **180***a* and the second drain electrode layer **180***b* as long as the second source electrode layer **180***a* and the second drain electrode layer **180***b* are provided in this manner at least over part of a region of the oxide semiconductor layer **106** serving as a channel. Note that when the first source electrode layer and the first drain electrode layer are covered with the second source electrode layer and the second drain electrode layer as in any of the transistors described in the above embodiments, a possibility that oxygen might be diffused or transferred to the side faces of the first source electrode layer and the first drain electrode layer is reduced; accordingly, with such a structure, oxygen can be favorably supplied to the oxide semiconductor layer from the oxide insulating film through the gate insulating film.

The above is the transistor of one embodiment of the present invention, whose structure can suppress an increase in oxygen vacancies in the oxide semiconductor layer. Specifically, in the transistor, oxygen can be supplied from the oxide insulating film and the gate insulating film which are in contact with the oxide semiconductor layer to the oxide semiconductor layer. It is thus possible to provide a semiconductor device having favorable electrical characteristics and high long-term reliability.

Note that this embodiment can be combined as appropriate with any of the other embodiments and examples in this specification.

Embodiment 6

In this embodiment, an example of a semiconductor device (memory device) which includes a transistor of one embodiment of the present invention, which can retain stored data even when not powered, and which has an unlimited number of write cycles will be described with reference to drawings.

FIG. **11**A is a cross-sectional view of the semiconductor device, and FIG. **11**B is a circuit diagram of the semiconductor device.

The semiconductor device illustrated in FIGS. **11**A and **11**B includes a transistor **3200** including a first semiconductor material in a lower portion, and a transistor **3202** including a second semiconductor material and a capacitor **3204** in an upper portion. As the transistor **3202**, any of the transistors described in Embodiments 1 to 5 can be used, and an example in which the transistor **150** described in Embodiment 1 with reference to FIGS. **1**A to **1**E is applied to the transistor **3202** is described in this embodiment. One electrode of the capacitor **3204** is formed using the same material as a gate electrode of the transistor **3202**, the other electrode thereof is formed using the same material as a source electrode and a drain electrode of the transistor **3202**, and a dielectric thereof is formed using the same material as the a gate insulating film **112** of the transistor **3202**; thus, the capacitor **3204** can be formed concurrently with the transistor **3202**.

Here, the first semiconductor material and the second semiconductor material are preferably materials having different band gaps. For example, the first semiconductor material may be a semiconductor material (such as silicon) other than an oxide semiconductor, and the second semiconductor material may be the oxide semiconductor described in Embodiment 1. A transistor including, for example, crystalline silicon as a material other than an oxide semiconductor can operate at high speed easily. On the other hand, a transistor including an oxide semiconductor enables charge to be stored for a long time owing to its electrical characteristics, that is, the low off-state current.

Although both of the above transistors are n-channel transistors in the following description, it is needless to say that p-channel transistors can be used. The specific structure of the semiconductor device, such as the material used for the semiconductor device and the structure of the semiconductor device, is not necessarily limited to those described here except for the use of the transistor described in Embodiment 1, which is formed using an oxide semiconductor for holding data.

The transistor **3200** in FIG. **11**A includes a channel formation region provided in a substrate **3000** including a semiconductor material (such as crystalline silicon), impurity regions provided such that the channel formation region is sandwiched therebetween, intermetallic compound regions provided in contact with the impurity regions, a gate insulating film provided over the channel formation region, and a gate electrode layer provided over the gate insulating film. Note that a transistor whose source electrode layer and drain electrode layer are not illustrated in a drawing may be referred to as a transistor for the sake of convenience. Further, in such a case, in description of a connection of a transistor, a source region and a source electrode layer may be collectively referred to as a source electrode layer, and a drain region and a drain electrode layer may be collectively referred to as a drain electrode layer. That is, in this specification, the term "source electrode layer" may include a source region.

Further, an element isolation insulating layer **3106** is formed on the substrate **3000** so as to surround the transistor **3200**, and an oxide insulating film **3220** is formed so as to cover the transistor **3200**. The element isolation insulating layer **3106** can be formed by an element isolation technique such as local oxidation of silicon (LOCOS) or shallow trench isolation (STI).

For example, the transistor **3200** formed using a crystalline silicon substrate can operate at high speed. Thus, when the transistor is used as a reading transistor, data can be read at a high speed. As treatment prior to formation of the transistor **3202** and the capacitor **3204**, CMP treatment is performed on the oxide insulating film **3220** covering the transistor **3200**, whereby the oxide insulating film **3220** is planarized and, at the same time, an upper surface of the gate electrode layer of the transistor **3200** is exposed.

The transistor **3202** is provided over the oxide insulating film **3220**, and one of the source electrode and the drain electrode thereof is extended so as to function as the other electrode of the capacitor **3204**.

The transistor **3202** in FIG. **11**A is a top-gate transistor in which a channel is formed in an oxide semiconductor layer. Since the off-state current of the transistor **3202** is low, stored data can be retained for a long time owing to such a transistor. In other words, refresh operation becomes unnecessary or the frequency of the refresh operation in a semiconductor memory device can be extremely low, which leads to a sufficient reduction in power consumption.

Further, an electrode **3150** overlaps with the transistor **3202** with the oxide insulating film **3220** provided therebetween. By supplying an appropriate potential to the electrode **3150**, the threshold voltage of the transistor **3202** can be controlled. In addition, long-term reliability of the transistor **3202** can be improved.

The transistor **3200** and the transistor **3202** can be formed so as to overlap with each other as illustrated in FIG. **11**A, whereby the area occupied by them can be reduced. Accordingly, the degree of integration of the semiconductor device can be increased.

An example of a circuit configuration corresponding to FIG. **11**A is illustrated in FIG. **11**B.

In FIG. **11**B, a first wiring (1st Line) is electrically connected to a source electrode layer of the transistor **3200**. A second wiring (2nd Line) is electrically connected to a drain electrode layer of the transistor **3200**. A third wiring (3rd Line) is electrically connected to one of the source and drain electrode layers of the transistor **3202**, and a fourth wiring (4th Line) is electrically connected to the gate electrode layer of the transistor **3202**. The gate electrode layer of the transistor **3200** and the other of the source and drain electrode layers of the transistor **3202** are electrically connected to the one electrode of the capacitor **3204**. A fifth wiring (5th Line) is electrically connected to the other electrode of the capacitor **3204**.

The semiconductor device in FIG. **11**B utilizes a characteristic in which the potential of the gate electrode layer of the transistor **3200** can be held, and thus enables writing, storing, and reading of data as follows.

Writing and holding of data will be described. First, the potential of the fourth wiring is set to a potential at which the transistor **3202** is turned on, so that the transistor **3202** is turned on. Accordingly, the potential of the third wiring is supplied to the gate electrode layer of the transistor **3200** and to the capacitor **3204**. That is, predetermined charge is supplied to the gate electrode layer of the transistor **3200** (writing). Here, one of two kinds of charges providing different potential levels (hereinafter referred to as a low-level charge and a high-level charge) is supplied. After that, the potential of the fourth wiring is set to a potential at which the transistor **3202** is turned off, so that the transistor **3202** is turned off. Thus, the charge supplied to the gate electrode layer of the transistor **3200** is held (holding).

Since the off-state current of the transistor **3202** is extremely low, the charge of the gate electrode layer of the transistor **3200** is held for a long time.

Next, reading of data is described. By supplying an appropriate potential (a reading potential) to the fifth wiring while supplying a predetermined potential (a constant potential) to the first wiring, the potential of the second wiring varies depending on the amount of charge held in the gate electrode layer of the transistor **3200**. This is because in general, when the transistor **3200** is an n-channel transistor, an apparent threshold voltage V_{th_H} in the case where the high-level charge is given to the gate electrode layer of the transistor **3200** is lower than an apparent threshold voltage V_{th_L} in the case where the low-level charge is given to the gate electrode layer of the transistor **3200**. Here, an apparent threshold voltage refers to the potential of the fifth wiring which is needed to turn on the transistor **3200**. Thus, the potential of the fifth wiring is set to a potential V_0 which is between V_{th_H} and V_{th_L}, whereby charge supplied to the gate electrode layer of the transistor **3200** can be determined. For example, in the case where the high-level charge is supplied in writing, when the potential of the fifth wiring is V_0 ($>V_{th\_H}$), the transistor **3200** is turned on. In the case where the low-level charge is supplied in writing, even when the potential of the fifth wiring is V_0 ($<V_{th\_L}$), the transistor **3200** remains off. Therefore, the data stored in the gate electrode layer can be read by determining the potential of the second wiring.

Note that in the case where memory cells are arrayed, it is necessary that only data of a desired memory cell be able to be read. The fifth wiring in the case where data is not read may be supplied with a potential at which the transistor **3200** is turned off regardless of the state of the gate electrode layer, that is, a potential lower than V_{th_H}. Alternatively, the fifth wiring may be supplied with a potential at which the transistor **3200** is turned on regardless of the state of the gate electrode layer, that is, a potential higher than V_{th_L}.

When a transistor having a channel formation region formed using an oxide semiconductor and having extremely low off-state current is applied to the semiconductor device in this embodiment, the semiconductor device can store data for an extremely long period. In other words, refresh operation becomes unnecessary or the frequency of the refresh operation can be extremely low, which leads to a sufficient reduction in power consumption. Moreover, stored data can be retained for a long period even when power is not supplied (note that a potential is preferably fixed).

Further, in the semiconductor device described in this embodiment, high voltage is not needed for writing data and there is no problem of deterioration of elements. For example, unlike a conventional nonvolatile memory, it is not necessary to inject and extract electrons into and from a floating gate, and thus a problem such as deterioration of a gate insulating film does not arise at all. That is, the semiconductor device according to the disclosed invention does not have a limitation on the number of times data can be rewritten, which is a problem of a conventional nonvolatile memory, and the reliability thereof is drastically improved. Furthermore, data is written depending on the on state and the off state of the transistor, whereby high-speed operation can be easily achieved.

As described above, a miniaturized and highly-integrated semiconductor device having high electrical characteristics and a manufacturing method of the semiconductor device can be provided.

Note that this embodiment can be combined as appropriate with any of the other embodiments and examples in this specification.

Embodiment 7

In this embodiment, a semiconductor device including a transistor of one embodiment of the present invention, which can retain stored data even when not powered, which does not have a limitation on the number of write cycles, and which has a structure different from that described in Embodiment 6 will be described.

FIG. **12**A illustrates an example of a circuit configuration of the semiconductor device, and FIG. **12**B is a conceptual diagram illustrating an example of the semiconductor device. As a transistor **4162** included in the semiconductor device, any of the transistors described in Embodiments 1 to 5 can be used. A capacitor **4254** can be formed through the same process and at the same time as the transistor **4162** in a manner similar to that of the capacitor **3204** described in Embodiment 6.

In the semiconductor device illustrated in FIG. **12**A, a bit line BL is electrically connected to a source electrode of the transistor **4162**, a word line WL is electrically connected to a gate electrode of the transistor **4162**, and a drain electrode of the transistor **4162** is electrically connected to a first terminal of the capacitor **4254**.

Next, writing and storing of data in the semiconductor device (a memory cell **4250**) illustrated in FIG. **12**A are described.

First, the potential of the word line WL is set to a potential at which the transistor **4162** is turned on, and the transistor **4162** is turned on. Accordingly, the potential of the bit line BL is supplied to the first terminal of the capacitor **4254** (writing). After that, the potential of the word line WL is set to a potential at which the transistor **4162** is turned off, so that the transistor **4162** is turned off. Thus, the potential at the first terminal of the capacitor **4254** is held (holding).

In addition, the transistor **4162** including an oxide semiconductor has an extremely low off-state current. For that reason, the potential of the first terminal of the capacitor **4254** (or a charge accumulated in the capacitor **4254**) can be held for an extremely long time by turning off the transistor **4162**.

Next, reading of data is described. When the transistor **4162** is turned on, the bit line BL which is in a floating state and the capacitor **4254** are electrically connected to each other, and the charge is redistributed between the bit line BL and the capacitor **4254**. As a result, the potential of the bit line BL is changed. The amount of change in potential of the bit line BL varies depending on the potential of the first terminal of the capacitor **4254** (or the charge accumulated in the capacitor **4254**).

For example, the potential of the bit line BL after charge redistribution is $(C_B \times V_{B0} + C \times V)/(C_B + C)$, where V is the potential of the first terminal of the capacitor **4254**, C is the capacitance of the capacitor **4254**, C_B is the capacitance of the bit line BL (hereinafter also referred to as bit line capacitance), and V_{B0} is the potential of the bit line BL before the charge redistribution. Therefore, it can be found that assuming that the memory cell **4250** is in either of two states in which the potentials of the first terminal of the capacitor **4254** are V_1 and V_0 ($V_1 > V_0$), the potential of the bit line BL in the case of holding the potential $V_1 (=(C_B \times V_{B0} + C \times V_1)/(C_B + C))$ is higher than the potential of the bit line BL in the case of holding the potential $V_0 (=(C_B \times V_{B0} + C \times V_0)/(C_B + C))$.

Then, by comparing the potential of the bit line BL with a predetermined potential, data can be read.

As described above, the semiconductor device illustrated in FIG. **12**A can hold charge that is accumulated in the capacitor **4254** for a long time because the off-state current of the transistor **4162** is extremely low. In other words, refresh operation becomes unnecessary or the frequency of the refresh operation can be extremely low, which leads to a sufficient reduction in power consumption. Moreover, stored data can be retained for a long period even when power is not supplied.

Next, the semiconductor device illustrated in FIG. **12**B is described.

The semiconductor device illustrated in FIG. **12**B includes a memory cell array **4251** (memory cell arrays **4251***a* and **4251***b*) including the plurality of memory cells **4250** illustrated in FIG. **12**A as memory circuits in the upper portion, and a peripheral circuit **4253** in the lower portion, which is necessary for operating the memory cell array **4251**. Note that the peripheral circuit **4253** is electrically connected to the memory cell array **4251**.

In the structure illustrated in FIG. **12**B, the peripheral circuit **4253** can be provided under the memory cell array **4251**. Thus, the size of the semiconductor device can be reduced.

It is preferable that a semiconductor material of the transistor provided in the peripheral circuit **4253** be different from that of the transistor **4162**. For example, silicon, germanium, silicon germanium, silicon carbide, or gallium arsenide can be used, and a single crystal semiconductor is preferably used. Alternatively, an organic semiconductor material or the like may be used. A transistor including such a semiconductor material can operate at sufficiently high speed. Thus, the transistor enables a variety of circuits (e.g., a logic circuit and a driver circuit) which need to operate at high speed to be favorably obtained.

Note that FIG. **12**B illustrates, as an example, the semiconductor device in which the memory cell array **4251** has a stack of the memory cell array **4251***a* and the memory cell array **4251***b*; however, the number of stacked memory cell arrays is not limited to two. For the memory cell array **4251**, a stack of three or more memory cell arrays may be used, or only one memory cell array may be used.

The transistor **4162** is formed using an oxide semiconductor, and any of the transistors described in Embodiments 1 to 5 can be used as the transistor **4162**. Since the off-state current of the transistor including an oxide semiconductor is low, stored data can be retained for a long time. In other words, the frequency of refresh operation can be extremely low, which leads to a sufficient reduction in power consumption.

A semiconductor device having a novel feature can be obtained by being provided with both a peripheral circuit which includes the transistor including a material other than an oxide semiconductor (in other words, a transistor capable of operating at sufficiently high speed) and a memory circuit which includes the transistor including an oxide semiconductor (in a broader sense, a transistor whose off-state current is sufficiently low). In addition, with a structure where the peripheral circuit and the memory circuit are stacked, an increase in the degree of integration of the semiconductor device can be achieved.

As described above, a miniaturized and highly-integrated semiconductor device having high electrical characteristics can be provided.

Note that this embodiment can be combined as appropriate with any of the other embodiments and examples in this specification.

Embodiment 8

In this embodiment, examples of an electronic device and an electric device which can use any of the transistors described in Embodiments 1 to 5 will be described.

Any of the transistors described in Embodiments 1 to 5 can be applied to a variety of electronic devices (including game machines) and electric devices. Examples of the electronic devices include display devices of televisions, monitors, and the like, lighting devices, desktop personal computers and notebook personal computers, word processors, image reproduction devices which reproduce still images or moving images stored in recording media such as digital versatile discs (DVDs), portable compact disc (CD) players, radio receivers, tape recorders, headphone stereos, stereos, cordless phone handsets, transceivers, mobile phones, car phones, portable game machines, calculators, portable information terminals, electronic notebooks, e-book readers, electronic translators, audio input devices, cameras such as video cameras and digital still cameras, electric shavers, and IC chips. Examples of the electric devices include high-frequency heating appliances such as microwave ovens, electric rice cookers, electric washing machines, electric vacuum cleaners, air-conditioning systems such as air conditioners, dishwashers, dish dryers, clothes dryers, futon dryers, electric refrigerators, electric freezers, electric refrigerator-freezers, freezers for preserving DNA, radiation counters, and medical equipment such as dialyzers. In addition, the examples include alarm devices such as smoke detectors, gas alarm devices, and security alarm devices. Further, the examples include industrial equipment such as guide lights, traffic lights, belt conveyors, elevators, escalators, industrial robots, and power storage systems. In addition, moving objects and the like driven by oil engines and electric motors using power from non-aqueous secondary batteries are also included in the category of electric devices. Examples of the moving objects include electric vehicles (EV), hybrid electric vehicles (HEV) which include both an internal-combustion engine and a motor, plug-in hybrid electric vehicles (PHEV), tracked vehicles in which caterpillar tracks are substituted for wheels of these vehicles, motorized bicycles including motor-assisted bicycles, motorcycles, electric wheelchairs, golf carts, boats or ships, submarines, helicopters, aircrafts, rockets, artificial satellites, space probes, planetary probes, and spacecrafts. Specific examples of these electronic devices and electric devices are illustrated in FIG. **13**, FIG. **14**, FIGS. **15**A to **15**C, and FIGS. **16**A to **16**C.

First, as an example of the alarm device, a structure of a fire alarm is described with reference to FIG. **13**. A fire alarm in this specification refers to any device which raises an alarm over fire occurrence instantly, and for example, a residential fire alarm, an automatic fire alarm system, and a fire detector used for the automatic fire alarm system are included in its category.

An alarm device illustrated in FIG. **13** includes at least a microcomputer **500**. Here, the microcomputer **500** is provided in the alarm device. The microcomputer **500** includes a power gate controller **503** electrically connected to a high potential power supply line VDD, a power gate **504** electrically connected to the high potential power supply line VDD and the power gate controller **503**, a CPU (central processing unit) **505** electrically connected to the power gate **504**, and a sensor portion **509** electrically connected to the power gate **504** and the CPU **505**. Further, the CPU **505** includes a volatile memory portion **506** and a nonvolatile memory portion **507**.

The CPU **505** is electrically connected to a bus line **502** through an interface **508**. The interface **508** as well as the CPU **505** is electrically connected to the power gate **504**. As a bus standard of the interface **508**, an I^2C bus can be used, for example. A light-emitting element **530** electrically connected to the power gate **504** through the interface **508** is provided in the alarm device described in this embodiment.

The light-emitting element **530** is preferably an element which emits light with high directivity, and for example, an organic EL element, an inorganic EL element, or a light-emitting diode (LED) can be used.

The power gate controller **503** includes a timer and controls the power gate **504** with use of the timer. The power gate **504** allows or stops supply of power from the high potential power supply line VDD to the CPU **505**, the sensor portion **509**, and the interface **508**, in accordance with the control by the power gate controller **503**. Here, as an example of the power gate **504**, a switching element such as a transistor can be given.

With use of the power gate controller **503** and the power gate **504**, power is supplied to the sensor portion **509**, the CPU **505**, and the interface **508** in a period during which the amount of light is measured, and supply of power to the sensor portion **509**, the CPU **505**, and the interface **508** can be stopped during an interval between measurement periods. The alarm device operates in such a manner, whereby power consumption can be reduced compared with the case where power is continuously supplied to the above structures.

In the case where a transistor is used as the power gate **504**, it is preferable to use a transistor which has an extremely low off-state current and is used for the nonvolatile memory portion **507**, for example, a transistor including an oxide semiconductor. With use of such a transistor, leakage current can be reduced when supply of power is stopped by the power gate **504**, so that a reduction in power consumption of the alarm device can be achieved.

A direct-current power source **501** may be provided in the alarm device described in this embodiment so that power is supplied from the direct-current power source **501** to the high potential power supply line VDD. An electrode of the direct-current power source **501** on a high potential side is electrically connected to the high potential power supply line VDD, and an electrode of the direct-current power source **501** on a low potential side is electrically connected to a low potential power supply line VSS. The low potential power supply line VSS is electrically connected to the microcomputer **500**. Here, the high potential power supply line VDD is supplied with a high potential H. The low potential power supply line VSS is supplied with a low potential L, for example, a ground potential (GND).

In the case where a battery is used as the direct-current power source **501**, for example, a battery case including an electrode electrically connected to the high potential power supply line VDD, an electrode electrically connected to the low potential power supply line VSS, and a housing which can hold the battery, is provided in a housing. Note that the alarm device described in this embodiment does not necessarily include the direct-current power source **501** and may have, for example, a structure in which power is supplied from an alternate-current power source provided outside the alarm device through a wiring.

As the above battery, a secondary battery such as a lithium ion secondary battery (also called a lithium ion storage battery or a lithium ion battery) can be used. Further, a solar battery is preferably provided to charge the secondary battery.

The sensor portion **509** measures a physical quantity relating to an abnormal situation and transmits a measurement value to the CPU **505**. A physical quantity relating to an abnormal situation depends on the usage of the alarm device, and in an alarm device functioning as a fire alarm, a physical quantity relating to a fire is measured. Accordingly, the sensor portion **509** measures the amount of light as a physical quantity relating to a fire and senses smoke.

The sensor portion **509** includes an optical sensor **511** electrically connected to the power gate **504**, an amplifier **512** electrically connected to the power gate **504**, and an AD converter **513** electrically connected to the power gate **504** and the CPU **505**. The optical sensor **511**, the amplifier **512**, and the AD converter **513** which are provided in the sensor portion **509**, and the light-emitting element **530** operate when the power gate **504** allows supply of power to the sensor portion **509**.

Here, FIG. **14** illustrates part of the cross section of the alarm device illustrated in FIG. **13**. In the alarm device, element isolation regions **603** are formed in a p-type semiconductor substrate **601**, and an n-channel transistor **719** including a gate insulating film **607**, a gate electrode layer **609**, n-type impurity regions **611***a* and **611***b*, an insulating film **615**, and an insulating film **617** is formed. The n-channel transistor **719** is formed using a semiconductor other than an oxide semiconductor, such as single crystal silicon, so that the n-channel transistor **719** can operate at sufficiently high speed. Accordingly, a volatile memory portion of a CPU that can achieve high-speed access can be formed.

In addition, contact plugs **619***a* and **619***b* are formed in openings which are formed by partly etching the insulating films **615** and **617**, and an insulating film **621** having groove portions is formed over the insulating film **617** and the contact plugs **619***a* and **619***b*.

Wirings **623***a* and **623***b* are formed in the groove portions of the insulating film **621**, and an insulating film **620** formed by a sputtering method, a CVD method, or the like is provided over the insulating film **621** and the wirings **623***a* and **623***b*. An insulating film **622** having a groove portion is formed over the insulating film **620**.

An electrode **624** functioning as a back gate electrode of a second transistor **717** is formed in the groove portion of the insulating film **622**. The electrode **624** can control the threshold voltage of the second transistor **717**.

An oxide insulating film **625** formed by a sputtering method, a CVD method, or the like is provided over the insulating film **622** and the electrode **624**, and the second transistor **717** and a photoelectric conversion element **714** are provided over the oxide insulating film **625**.

The second transistor **717** includes an oxide semiconductor layer **606**, a first source electrode layer **616***a* and a first drain electrode layer **616***b* in contact with the oxide semiconductor layer **606**, a second source electrode layer **626***a* and a second drain electrode layer **626***b* in contact with upper portions of the first source electrode layer **616***a* and the first drain electrode layer **616***b*, a gate insulating film **612**, a gate electrode layer **604**, and a protective insulating film **618**. Moreover, an insulating film **645** and an insulating film **646** cover the photoelectric conversion element **714** and the second transistor **717**, and a wiring **649** is formed over the insulating film **646** so as to be in contact with the first drain electrode layer **616***b*. The wiring **649** functions as the node which electrically connects a drain electrode of the second transistor **717** to the gate electrode layer **609** of the n-channel transistor **719**.

Although the structure in which the connection portion of the second transistor **717** and the wiring **649** is in contact with the first drain electrode layer **616***b* is shown as an example in this embodiment, without limitation thereon, a structure in which the connection portion is in contact with the second drain electrode layer **626***b* may be employed, for example.

Here, any of the transistors described in Embodiments 1 to 5 can be used as the second transistor **717**, and the oxide semiconductor layer **606** corresponds to the oxide semiconductor layer **106** described in Embodiment 1. Moreover, the first source electrode layer **616***a* and the first drain electrode layer **616***b* correspond to the first source electrode layer **108***a* and the first drain electrode layer **108***b* described in Embodiment 1, respectively. The second source electrode layer **626***a* and the second drain electrode layer **626***b* correspond to the second source electrode layer **110***a* and the second drain electrode layer **110***b* described in Embodiment 1, respectively.

The optical sensor **511** includes the photoelectric conversion element **714**, a capacitor, a first transistor, the second transistor **717**, a third transistor, and the n-channel transistor **719**. As the photoelectric conversion element **714**, a photodiode can be used here, for example.

One of terminals of the photoelectric conversion element **714** is electrically connected to the low potential power supply line VSS, and the other of the terminals thereof is electrically connected to one of the first source electrode layer **616***a* and the first drain electrode layer **616***b* and/or one of the second source electrode layer **626***a* and the second drain electrode layer **626***b* of the second transistor **717**.

The gate electrode layer **604** of the second transistor **717** is supplied with an electric charge accumulation control signal Tx, and the other of the first source electrode layer **616***a* and the first drain electrode layer **616***b* and/or the other of the second source electrode layer **626***a* and the second drain electrode layer **626***b* of the second transistor **717** are/is electrically connected to one of a pair of electrodes of the capacitor, one of a source electrode and a drain electrode of the first transistor, and the gate electrode of the n-channel transistor **719** (hereinafter the node is referred to as a node FD in some cases).

The other of the pair of electrodes of the capacitor is electrically connected to the low potential power supply line VSS. A gate electrode of the first transistor is supplied with a reset signal Res, and the other of the source electrode and the drain electrode thereof is electrically connected to the high potential power supply line VDD.

One of a source electrode and a drain electrode of the n-channel transistor **719** is electrically connected to one of a source electrode and a drain electrode of the third transistor and the amplifier **512**. The other of the source electrode and the drain electrode of the n-channel transistor **719** is electrically connected to the high potential power supply line VDD. A gate electrode of the third transistor is supplied with a bias signal Bias, and the other of the source electrode and the drain electrode thereof is electrically connected to the low potential power supply line VSS.

Note that the capacitor is not necessarily provided. For example, in the case where parasitic capacitance of the n-channel transistor **719** or the like is sufficiently large, a structure without the capacitor may be employed.

Further, as each of the first transistor and the second transistor **717**, the transistor having an extremely low off-state current is preferably used. As the transistor having an extremely low off-state current, a transistor including an oxide semiconductor is preferably used. With such a structure, the potential of the node FD can be held for a long time.

In the structure in FIG. **14**, the photoelectric conversion element **714** is electrically connected to the second transistor **717** and is provided over the oxide insulating film **625**.

The photoelectric conversion element **714** includes a semiconductor film **660** provided over the oxide insulating film **625**, and the first source electrode layer **616***a* and an electrode **616***c* which are in contact with a top surface of the semiconductor film **660**. The first source electrode layer **616***a* is an electrode functioning as the source electrode or the drain electrode of the second transistor **717** and electrically connects the photoelectric conversion element **714** to the second transistor **717**. In the photoelectric conversion element **714**, the second source electrode layer **626***a* and an electrode **626***c* are provided over the first source electrode layer **616***a* and the electrode **616***c*, respectively.

Over the semiconductor film **660**, the second source electrode layer **626***a*, and the electrode **626***c*, the gate insulating film **612**, the protective insulating film **618**, the insulating film **645**, and the insulating film **646** are provided. Further, a wiring **656** is formed over the insulating film **646** and is in contact with the electrode **616***c* through an opening provided in the electrode **626***c*, the gate insulating film **612**, the protective insulating film **618**, the insulating film **645**, and the insulating film **646**.

The electrode **616***c* can be formed in steps similar to those of the first source electrode layer **616***a* and the first drain electrode layer **616***b*, and the wiring **656** can be formed in steps similar to those of the wiring **649**.

As the semiconductor film **660**, a semiconductor film which can perform photoelectric conversion is provided, and for example, silicon or germanium can be used. In the case of using silicon, the semiconductor film **660** functions as an optical sensor which senses visible light. Further, there is a difference, between silicon and germanium, in wavelengths of electromagnetic waves that can be absorbed. When the semiconductor film **660** includes germanium, a sensor which mainly senses an infrared ray can be obtained.

In the above manner, the sensor portion **509** including the optical sensor **511** can be incorporated into the microcomputer **500**, so that the number of components can be reduced and the size of the housing of the alarm device can be reduced. Note that in the case where the place of the optical sensor or the photoelectric conversion element needs a high degree of freedom, the optical sensor or the photoelectric conversion element may be externally provided so as to be electrically connected to the microcomputer **500**.

In the alarm device including the above-described IC chip, the CPU **505** in which a plurality of circuits including any of the transistors described in the above embodiments are combined and mounted on one IC chip is used.

FIGS. **15**A to **15**C are block diagrams illustrating a specific configuration of a CPU at least partly including any of the transistors described in Embodiments 1 to 5.

The CPU illustrated in FIG. **15**A includes an arithmetic logic unit (ALU) **1191**, an ALU controller **1192**, an instruction decoder **1193**, an interrupt controller **1194**, a timing controller **1195**, a register **1196**, a register controller **1197**, a bus interface (Bus I/F) **1198**, a rewritable ROM **1199**, and an ROM interface (ROM I/F) **1189** over a substrate **1190**. A semiconductor substrate, an SOI substrate, a glass substrate, or the like is used as the substrate **1190**. The ROM **1199** and the ROM interface **1189** may be provided over a separate chip. Needless to say, the CPU in FIG. **15**A is just an example in which the configuration has been simplified, and an actual CPU may have various configurations depending on the application.

An instruction that is input to the CPU through the bus interface **1198** is input to the instruction decoder **1193** and decoded therein, and then, input to the ALU controller **1192**, the interrupt controller **1194**, the register controller **1197**, and the timing controller **1195**.

The ALU controller **1192**, the interrupt controller **1194**, the register controller **1197**, and the timing controller **1195** conduct various controls in accordance with the decoded instruction. Specifically, the ALU controller **1192** generates signals for controlling the operation of the ALU **1191**. While the CPU is executing a program, the interrupt controller **1194** judges an interrupt request from an external input/output device or a peripheral circuit on the basis of its priority or a mask state, and processes the request. The register controller **1197** generates an address of the register **1196**, and reads/writes data from/to the register **1196** in accordance with the state of the CPU.

The timing controller **1195** generates signals for controlling operation timings of the ALU **1191**, the ALU controller **1192**, the instruction decoder **1193**, the interrupt controller **1194**, and the register controller **1197**. For example, the timing controller **1195** includes an internal clock generator for generating an internal clock signal CLK**2** based on a reference clock signal CLK**1**, and supplies the internal clock signal CLK**2** to the above circuits.

In the CPU illustrated in FIG. **15**A, a memory cell is provided in the register **1196**. As the memory cell of the register **1196**, any of the transistors described in the above embodiments can be used.

In the CPU illustrated in FIG. **15**A, the register controller **1197** selects operation of storing data in the register **1196** in accordance with an instruction from the ALU **1191**. That is, the register controller **1197** selects whether data is stored by a flip-flop or by a capacitor in the memory cell included in the register **1196**. When data storing by the flip-flop is selected, a power supply voltage is supplied to the memory cell in the register **1196**. When data storing by the capacitor is selected, the data is rewritten in the capacitor, and supply of power supply voltage to the memory cell in the register **1196** can be stopped.

The power supply can be stopped by a switching element provided between a memory cell group and a node to which a power supply potential VDD or a power supply potential VSS is supplied, as illustrated in FIG. **15**B or FIG. **15**C. Circuits illustrated in FIGS. **15**B and **15**C are described below.

FIGS. **15**B and **15**C each illustrate an example of the configuration of a memory circuit in which any of the transistors described in the above embodiments is used as a switching element which controls supply of a power supply potential to a memory cell.

The memory device illustrated in FIG. **15**B includes a switching element **1141** and a memory cell group **1143** including a plurality of memory cells **1142**. Specifically, as each of the memory cells **1142**, any of the transistors described in the above embodiments can be used. Each of the memory cells **1142** included in the memory cell group **1143** is supplied with the high-level power supply potential VDD via the switching element **1141**. Further, each of the memory cells **1142** included in the memory cell group **1143** is supplied with a potential of a signal IN and the low-level power supply potential VSS.

In FIG. **15**B, any of the transistors described in the above embodiments is used as the switching element **1141**, and the switching of the transistor is controlled by a signal SigA supplied to a gate electrode layer thereof.

Note that FIG. **15**B illustrates the configuration in which the switching element **1141** includes only one transistor; however, without particular limitation thereon, the switching element **1141** may include a plurality of transistors. In the case where the switching element **1141** includes a plurality of transistors which function as switching elements, the plurality of transistors may be connected to each other in parallel, in series, or in combination of parallel connection and series connection.

Although the switching element **1141** controls the supply of the high-level power supply potential VDD to each of the memory cells **1142** included in the memory cell group **1143** in FIG. **15**B, the switching element **1141** may control the supply of the low-level power supply potential VSS.

In FIG. **15**C, an example of a memory device in which each of the memory cells **1142** included in the memory cell group **1143** is supplied with the low-level power supply potential VSS via the switching element **1141** is illustrated. The supply of the low-level power supply potential VSS to each of the memory cells **1142** included in the memory cell group **1143** can be controlled by the switching element **1141**.

When a switching element is provided between a memory cell group and a node to which the power supply potential VDD or the power supply potential VSS is supplied, data can be stored even in the case where an operation of a CPU is temporarily stopped and the supply of the power supply voltage is stopped; accordingly, power consumption can be reduced. Specifically, for example, while a user of a personal computer does not input data to an input device such as a keyboard, the operation of the CPU can be stopped, so that the power consumption can be reduced.

Although the CPU is given as an example here, the transistor can also be applied to an LSI such as a digital signal processor (DSP), a custom LSI, or a field programmable gate array (FPGA).

In FIG. **16**A, an alarm device **8100** is a residential fire alarm, which is an example of an electric device including a sensor portion and a microcomputer **8101**. Note that the microcomputer **8101** is an example of an electronic device including a CPU in which any of the transistors described in the above embodiments is used.

In FIG. **16**A, an air conditioner which includes an indoor unit **8200** and an outdoor unit **8204** is an example of an electric device including the CPU in which any of the transistors described in the above embodiments is used. Specifically, the indoor unit **8200** includes a housing **8201**, an air outlet **8202**, a CPU **8203**, and the like. Although the CPU **8203** is provided in the indoor unit **8200** in FIG. **16**A, the CPU **8203** may be provided in the outdoor unit **8204**. Alternatively, the CPU **8203** may be provided in both the indoor unit **8200** and the outdoor unit **8204**. By using any of the transistors described in the above embodiments as the CPU in the air conditioner, a reduction in power consumption of the air conditioner can be achieved.

In FIG. **16**A, an electric refrigerator-freezer **8300** is an example of an electric device including the CPU in which any of the transistors described in the above embodiments is used. Specifically, the electric refrigerator-freezer **8300** includes a housing **8301**, a door for a refrigerator **8302**, a door for a freezer **8303**, a CPU **8304**, and the like. In FIG. **16**A, the CPU **8304** is provided in the housing **8301**. When any of the transistors described in the above embodiments is used as the CPU **8304** of the electric refrigerator-freezer **8300**, a reduction in power consumption of the electric refrigerator-freezer **8300** can be achieved.

FIGS. **16**B and **16**C illustrate an example of an electric vehicle which is an example of an electric device. An electric vehicle **9700** is equipped with a secondary battery **9701**. The output of the electric power of the secondary battery **9701** is adjusted by a control circuit **9702** and the electric power is supplied to a driving device **9703**. The control circuit **9702** is controlled by a processing unit **9704** including a ROM, a RAM, a CPU, or the like which is not illustrated. When any of the transistors described in the above embodiments is used as the CPU in the electric vehicle **9700**, a reduction in power consumption of the electric vehicle **9700** can be achieved.

The driving device **9703** includes a DC motor or an AC motor either alone or in combination with an internal-combustion engine. The processing unit **9704** outputs a control signal to the control circuit **9702** based on input data such as data of operation (e.g., acceleration, deceleration, or stop) by a driver or data during driving (e.g., data on an upgrade or a downgrade, or data on a load on a driving wheel) of the electric vehicle **9700**. The control circuit **9702** adjusts the electric energy supplied from the secondary battery **9701** in accordance with the control signal of the processing unit **9704** to control the output of the driving device **9703**. In the case where the AC motor is mounted, although not illustrated, an inverter which converts direct current into alternate current is also incorporated.

Note that this embodiment can be combined as appropriate with any of the other embodiments and examples in this specification.

EXAMPLE 1

In this example, a conductive film was formed over an oxide semiconductor film and diffusion or transfer of elements which exist between the stacked films was examined by secondary ion mass spectrometry (SIMS), and results thereof will be described.

FIGS. **17**A and **17**B each show SIMS analysis results of profiles of an oxygen isotope (^{18}O) in a depth direction before and after heat treatment in samples which were each fabricated with a stack of an IGZO film and a tungsten film by a sputtering method. Note that the IGZO film was formed by a DC sputtering method with a sputtering target containing In, Ga, and Zn at an atomic ratio of 1:1:1 or 1:3:2 and a deposition gas containing Ar and O_2 (^{18}O) at a flow rate ratio of 2:1. The tungsten film was formed by a DC sputtering method with a tungsten sputtering target and a 100 percent Ar gas used as a deposition gas. Note that heat treatment was performed at 300° C., 350° C., 400° C., and 450° C. each for one hour, and five samples including a sample which was not subjected to heat treatment were compared with one another.

Here, the IGZO film formed with the sputtering target containing In, Ga, and Zn at an atomic ratio of 1:1:1 is a crystalline IGZO film, and the IGZO film formed with the sputtering target containing In, Ga, and Zn at an atomic ratio of 1:3:2 is an amorphous IGZO film.

As shown in FIGS. **17**A and **17**B, as the temperature of the heat treatment is increased, oxygen of the oxide semiconductor film is taken into the tungsten film despite the composition or crystallinity of the oxide semiconductor film.

Since the fabrication process of the transistor involves some heat treatment steps, oxygen vacancies are generated in a region of the oxide semiconductor layer, which is in contact with the source electrode or the drain electrode, and the region becomes an n-type. Thus, the n-type region can serve as a source or a drain of the transistor.

FIGS. **18**A and **18**B each show the SIMS analysis results in samples which were each fabricated using a tantalum nitride film instead of the tungsten film. The tantalum nitride film was formed by a reactive sputtering method (a DC sputtering method) with a tantalum sputtering target and a deposition gas containing Ar and N_2 at a flow rate ratio of 5:1. Note that heat treatment was performed under four conditions similar to the above, and five samples including a sample which was not subjected to heat treatment were compared with one another.

FIG. **18**A shows the SIMS analysis results in samples which were each fabricated with a stack of the IGZO film whose atomic ratio of In to Ga and Zn was 1:1:1 and the tantalum nitride film. In any of the samples, transfer of oxygen to the tantalum nitride film was not observed and its behavior was different from that of the sample with the tungsten film in FIG. **17**A. FIG. **18**B shows the SIMS analysis results in samples which were each fabricated with a stack of the IGZO film whose atomic ratio of In to Ga and Zn was 1:3:2 and the tantalum nitride film. In any of the samples, transfer of oxygen to the tantalum nitride film was not observed and its behavior was different from that of the sample with the tungsten film in FIG. **17**B. Accordingly, it can be said that the tantalum nitride film is a film that is not easily bonded to oxygen or a film to which oxygen is not easily transferred.

FIGS. **19**A and **19**B each show the SIMS analysis results in samples which were each fabricated using a titanium nitride film instead of the tungsten film. The titanium nitride film was formed by a reactive sputtering method (a DC sputtering method) with a titanium sputtering target and a 100 percent N_2 gas used as a deposition gas. Note that heat treatment was performed under four conditions similar to the above, and five samples including a sample which was not subjected to heat treatment were compared with one another.

FIG. **19**A shows the SIMS analysis results in samples which were each fabricated with a stack of the IGZO film whose atomic ratio of In to Ga and Zn was 1:1:1 and the titanium nitride film. In either sample, transfer of oxygen to the titanium nitride film was not observed and its behavior was different from that of the sample with the tungsten film in FIG. **17**A. FIG. **19**B shows the SIMS analysis results in samples which were each fabricated with a stack of the IGZO film whose atomic ratio of In to Ga and Zn was 1:3:2 and the titanium nitride film. In either sample, transfer of oxygen to the titanium nitride film was not observed and its behavior was different from that of the sample with the tungsten film in FIG. **17**B. Accordingly, it can be said that the titanium nitride film is a film that is not easily bonded to oxygen or a film to which oxygen is not easily transferred.

Next, transfer of an impurity to an IGZO film was examined by SIMS analysis, and results thereof are described.

FIGS. **20**A and **20**B each show SIMS analysis results of profiles of nitrogen in a depth direction before and after heat treatment in samples which were each fabricated with a tantalum nitride film or a titanium nitride film formed over an IGZO film by a sputtering method. Note that the IGZO film was formed by a DC sputtering method with a sputtering target containing In, Ga, and Zn at an atomic ratio of 1:1:1 and a deposition gas containing Ar and O_2 at a flow rate ratio of 2:1. The tantalum nitride film and the titanium nitride film were formed by the above method. Note that heat treatment was performed at 400° C. for one hour, and two samples including a sample which was not subjected to heat treatment were compared with each other.

As shown in FIGS. **20**A and **20**B, in either sample, transfer of nitrogen to the IGZO film was not observed. Therefore, nitrogen which serves as a donor in the IGZO film is not widely transferred to the IGZO film from the tantalum nitride film or the titanium nitride film; accordingly, a channel formation region of the transistor is not made to have n-type conductivity.

FIGS. **21**A and **21**B show SIMS analysis results of profiles of tantalum and titanium, respectively, in a depth direction in samples similar to those shown in FIGS. **20**A and **20**B as examples. As shown in FIGS. **21**A and **21**B, transfer of tantalum or titanium to the IGZO film was not observed. Accordingly, each of titanium and tantalum which might serve as an impurity affecting the electrical characteristics of the transistor is not widely transferred to the IGZO film from the tantalum nitride film or the titanium nitride film.

The above results showed that a film of a conductive nitride such as tantalum nitride or titanium nitride is a film that is not easily bonded to oxygen or a film to which oxygen is not easily transferred, and nitrogen and a metal element in such a conductive nitride are not easily transferred to the oxide semiconductor film.

Note that this example can be combined as appropriate with any of embodiments or the other example in this specification.

EXAMPLE 2

In this example, measurement results of sheet resistance values of an oxide semiconductor film after removal of a conductive film which was formed over the oxide semiconductor film will be described.

FIG. **22** shows measurement results of sheet resistance values of samples each fabricated as follows with respect to a depth to which an IGZO film was etched: the IGZO film was formed by a sputtering method, a tungsten film or a titanium nitride film was stacked over the IGZO film by a sputtering method, and then the tungsten film or the titanium nitride film was removed. For comparison, a sample in which a conductive film was not formed over the IGZO film was also fabricated. Note that the IGZO film was formed by a DC sputtering method with a sputtering target containing In, Ga, and Zn at an atomic ratio of 1:1:1 and a deposition gas containing Ar and O_2 (^{18}O) at a flow rate ratio of 2:1. The tungsten film was formed by a DC sputtering method with a tungsten sputtering target and a 100 percent Ar gas used as a deposition gas. The titanium nitride film was formed by a reactive sputtering method (a DC sputtering method) with a titanium sputtering target and a 100 percent N_2 gas used as a deposition gas. The tungsten film and the titanium nitride film were etched using hydrogen peroxide water. The IGZO film was etched using a mixed solution of hydrogen peroxide water and ammonia. The remaining thickness of the IGZO film after the etching was measured using spectroscopic ellipsometry before and after the etching to obtain the depth to which the IGZO film was etched.

In the sample in which the tungsten film was formed over the IGZO film, the resistance of a region of the IGZO film, which was formed to a depth of about 5 nm from the surface of the IGZO film, was reduced as shown in FIG. **22**. This suggests that a low-resistant mixed layer of IGZO and tungsten is formed in a region of the IGZO film, which is close to the surface thereof, and that an n-type region is formed due to oxygen vacancies which exist in the above region by transfer of oxygen of the IGZO film to the tungsten film, for example.

On the other hand, in the sample in which the titanium nitride film was formed over the IGZO film and the sample in which a conductive film was not formed over the IGZO film, the resistance of each of the IGZO films was not reduced. This suggests that elements of titanium nitride are not easily transferred to the IGZO film and that oxygen of the IGZO film is not easily transferred to the titanium nitride film, for example.

FIG. **23**A shows measurement results of sheet resistance values of samples each fabricated as follows with respect to a depth to which an IGZO film was etched: the IGZO film was formed by a sputtering method, a tungsten film or a titanium nitride film was stacked over the IGZO film by a sputtering method, heat treatment was performed, and then the tungsten film or the titanium nitride film was removed. For comparison, a sample in which a conductive film was not formed over the IGZO film was also fabricated. Note that the formation of the IGZO film, and the tungsten film or the titanium nitride film and the removal of the tungsten film or the titanium nitride film were performed in manners similar to those of the above. The heat treatment was performed at 400° C. in a N_2 atmosphere for one hour.

As shown in FIG. **23**A, in any of the samples, the resistance of the IGZO film was reduced. Here, in the sample in which the tungsten film was formed over the IGZO film, the IGZO film in a region close to a surface thereof has the lowest resistance, and a reduction in resistance proceeded up to the greatest depth as compared with the case of the other samples. This suggests that the tungsten film takes oxygen of the IGZO film thereinto most easily. Further, the behavior of the sample in which the titanium nitride film was formed over the IGZO film was similar to that of the sample in which a conductive film was not formed over the IGZO film. In other words, in the sample in which the tungsten film was formed over the IGZO film, the resistance of the IGZO film was reduced by transfer of oxygen of the IGZO film to the tungsten film, whereas in the sample in which the titanium nitride film was formed over the IGZO film, oxygen released from the IGZO film was transmitted through the titanium nitride film and released to the upper side. This result well accords with the SIMS analysis results shown in Example 1.

FIG. **23**B shows measurement results of sheet resistance values of samples each fabricated as follows with respect to a depth to which an IGZO film was etched: a silicon oxide film was formed by a sputtering method, the IGZO film was formed over the silicon oxide film by a sputtering method, a tungsten film or a titanium nitride film was stacked over the IGZO film by a sputtering method, heat treatment was performed, and then the tungsten film or the titanium nitride film was removed. For comparison, a sample in which a conductive film was not formed over the IGZO film was also fabricated. The silicon oxide film was formed by a reactive sputtering method (a DC sputtering method) with a silicon sputtering target and a 100 percent O_2 gas used as a deposition gas. Note that the formation of the IGZO film, and the tungsten film or the titanium nitride film and the removal of the tungsten film or the titanium nitride film were performed in manners similar to those of the above. The heat treatment was performed at 400° C. in a N_2 atmosphere for one hour.

As shown in FIG. **23**B, low-resistance regions in the IGZO film when seen in a thickness direction were smaller than those observed from the results shown in FIG. **23**A. This suggests that oxygen was supplied from the silicon oxide film to the IGZO film by the heat treatment and oxygen vacancies in the IGZO film were reduced; accordingly, the resistance of the IGZO film was increased. With use of a film which is capable of releasing oxygen and provided below the IGZO film in this manner, the thickness of a region of the IGZO film, whose resistance is reduced, can be controlled.

As described above, there were the following findings. A conductive film such as a tungsten film, which easily takes oxygen thereinto, is formed in contact with an IGZO film, so that the resistance of a region of the IGZO film, which is in contact with and close to the conductive film, can be reduced. Moreover, the region of the IGZO film, whose resistance is reduced, can be increased in a depth direction by heat treatment. Further, a film capable of releasing oxygen is formed close to the IGZO film, whereby the thickness of the region whose resistance is reduced can be controlled.

Note that this example can be combined as appropriate with any of embodiments or the other example in this specification.

This application is based on Japanese Patent Application serial no. 2012-230364 filed with Japan Patent Office on Oct. 17, 2012, the entire contents of which are hereby incorporated by reference.

What is claimed is:

1. A method for manufacturing a semiconductor device, including the steps of:

forming an oxide semiconductor layer over an oxide insulating film;

forming a first source electrode layer and a first drain electrode layer in contact with the oxide semiconductor layer by a first etching;

forming a conductive film over the first source electrode layer and the first drain electrode layer;

forming a resist mask over the conductive film by performing electron beam exposure;

forming a second source electrode layer and a second drain electrode layer covering the first source electrode layer and the first drain electrode layer, respectively, and being in contact with the oxide semiconductor layer by a second etching that etches the conductive film using the resist mask;

forming a gate insulating film over the oxide insulating film, the oxide semiconductor layer, the second source electrode layer, and the second drain electrode layer;

introducing oxygen into the gate insulating film; and

supplying the oxygen of the gate insulating film to the oxide semiconductor layer.

2. The method for manufacturing a semiconductor device according to claim **1**, wherein the introduction of oxygen into the gate insulating film is performed by an ion implantation method.

3. The method for manufacturing a semiconductor device according to claim **1**, further comprising the step of:

forming a gate electrode over the gate insulating film before oxygen is introduced into the gate insulating film.

4. The method for manufacturing a semiconductor device according to claim **1**, further comprising the steps of:

forming a gate electrode over the gate insulating film before oxygen is introduced into the gate insulating film; and

forming a protective insulating film over the gate electrode.

5. The method for manufacturing a semiconductor device according to claim **1**, wherein the first source electrode layer and the first drain electrode layer comprise at least one material selected from Al, Cr, Cu, Ta, Ti, Mo, and W.

6. The method for manufacturing a semiconductor device according to claim **1**, wherein the second source electrode layer and the second drain electrode layer comprise at least one material selected from tantalum nitride, titanium nitride, and ruthenium.

7. The method for manufacturing a semiconductor device according to claim **1**, wherein the second source electrode layer and the second drain electrode layer are in contact with the oxide insulating film.

8. A method for manufacturing a semiconductor device, including the steps of:

forming an oxide semiconductor layer over an oxide insulating film;

forming a first source electrode layer and a first drain electrode layer in contact with the oxide semiconductor layer by a first etching;

forming a conductive film over the first source electrode layer and the first drain electrode layer;

forming a resist mask over the conductive film by performing electron beam exposure;

forming a second source electrode layer and a second drain electrode layer covering the first source electrode layer and the first drain electrode layer, respectively, and being in contact with the oxide semiconductor layer by a second etching that etches the conductive film using the resist mask;

forming a gate insulating film over the oxide insulating film, the oxide semiconductor layer, the second source electrode layer, and the second drain electrode layer;

introducing oxygen into the gate insulating film; and

supplying the oxygen of the gate insulating film and the oxide insulating film to the oxide semiconductor layer.

9. The method for manufacturing a semiconductor device according to claim 8, wherein the introduction of oxygen into the gate insulating film is performed by an ion implantation method.

10. The method for manufacturing a semiconductor device according to claim 8, further comprising the step of:

forming a gate electrode over the gate insulating film before oxygen is introduced into the gate insulating film.

11. The method for manufacturing a semiconductor device according to claim 8, further comprising the steps of:

forming a gate electrode over the gate insulating film before oxygen is introduced into the gate insulating film; and

forming a protective insulating film over the gate electrode.

12. The method for manufacturing a semiconductor device according to claim 8, wherein the first source electrode layer and the first drain electrode layer comprise at least one material selected from Al, Cr, Cu, Ta, Ti, Mo, and W.

13. The method for manufacturing a semiconductor device according to claim 8, wherein the second source electrode layer and the second drain electrode layer comprise at least one material selected from tantalum nitride, titanium nitride, and ruthenium.

14. The method for manufacturing a semiconductor device according to claim 8, wherein the second source electrode layer and the second drain electrode layer are in contact with the oxide insulating film.

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